STIC Search Report
EIC 2800

STIC Database Tracking Number: 102612

TO:	From:
Thanhha S Pham **Location: CP4 4D14** **Art Unit : 2813** **Thursday, August 28, 2003** **Case Serial Number: 09/945436**	**Irina Speckhard** **Location: EIC 2800** **CP4-9C18** **Phone: 308-6559** **irina.speckhard@uspto.gov**

Search Notes

Examiner Pham,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

Rush By Tues.

6482 102612

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/27/03 Serial # 9/945,436 Priority Application Date 9/4/01

Your Name Thanhha Pham Examiner # 77023

AU 2813 Phone 308-6177 Room CP4-4D14

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?
Circle: (USPT) DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. USpatents 5,904,546 6,046,101 6,043,149 5,387,551

What types of references would you like? Please checkmark:

Primary Refs ___ Nonpatent Literature ___ Other _____
Secondary Refs ___ Foreign Patents ___
Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Planar anduction – substrate, passive regions b/t active regions
scribe line across passive region, passivation
layer over the ~~passive~~ active region, bond pad
– attaching glass panel on the passivation layer
– 1st cutting the substrate, 1st cutting partially or
incompletely penetrate the ~~substrate~~
– 2nd cutting / removing substrate material from passivation
regen in and surface of substrate, 2nd cutting / removing
exposing bond pad on surface of passive region
– cutting the glass panel in alignment with scribe line

Staff Use Only
Searcher: Jack Kpel
Searcher Phone: _____
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 8/27/03
Date Completed: 8/28/03
Searcher Prep/Rev Time: 170
Online Time: 70

Type of Search
Structure (#)_____
Bibliographic ✓
Litigation_____
Fulltext_____
Patent Family_____
Other_____

Vendors
STN ✓
Dialog ✓
Questel/Orbit_____
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 28aug03 10:16:52 User267149 Session D952.1

SYSTEM:OS  - DIALOG OneSearch
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         (c)2003 Japan Science and Tech Corp(JST)
  File  99:Wilson Appl. Sci & Tech Abs  1983-2003/Jul
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  File 144:Pascal  1973-2003/Aug W2
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  File 305:Analytical Abstracts  1980-2003/Aug W1
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removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2003/Jul
         (c) 2003 DECHEMA
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200355
         (c) 2003  Thomson Derwent
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Mar
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	1777	PLANAR???????(3N)INDUCT??????
S2	1330571	(INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?)) OR IC OR CHIP? ?
S3	1128853	HIGH??????(3N)(PERFORM??????? OR FREQUEN??????)
S4	46540	SUBSTRATE? ?(3N)(PASSIV???????? OR ACTIV????????)
S5	80421	REGION? ?(3N)(ACTIV???????? OR PASSIV????????)
S6	439027	(FIRST OR ONE OR SECOND OR TWO)(3N)SURFACE? ?
S7	259148	SUBSTRATE? ?(3N)(SURFACE? ? OR REGION? ?)
S8	784203	S4:S7
S9	3172	SCRIB???????(3N)LINE? ?
S10	21	SCRIB??????(3N)PASSIV??????
S11	1247	(ALIGN???????? OR ARRANG?????? OR PARALLEL????? OR GLASS OR CUTTING OR CUT)(3N)SCRIB??????
S12	3871	S9:S11
S13	6853	CONDUCT???????(3N)(INTERCONNECT??????? OR INTER()CONNECT??-?????)
S14	20368	BOND????????(3N)PAD? ?
S15	2910	EXPOS????????(3N)BOND???????
S16	22721	S14:S15
S17	5352	ATTACH????????(3N)GLASS
S18	13127	GLASS(3N)(PANEL? ? OR PASSIV????????)
S19	18184	S17:S18
S20	131004	(FIRST OR ONE OR SECOND OR TWO)(3N)(CUTTING OR CUT OR REMOV???????)
S21	36429	(CUTTING OR CUT OR SLICE???? OR INCISE???? OR REMOV??????? OR PENETRAT??????)(3N)SUBSTRATE? ?
S22	165341	S20:S21
S23	9436	(CUTTING OR CUT OR SLICE???? OR INCISE???? OR PENETRAT????-???)(3N)(PARTIAL??????? OR INCOMPLETE????????)
S24	65287	S2 AND S3
S25	69	S24 AND S1
S26	3	S25 AND S8
S27	2	RD (unique items)
S28	66	S25 NOT S26
S29	0	S28 AND S12
S30	1	S28 AND S13
S31	65	S28 NOT S30
S32	0	S31 AND S16
S33	0	S31 AND S19
S34	1	S31 AND S22
S35	64	S31 NOT S34
S36	0	S35 AND S23
S37	1960	S24 AND S8
S38	2	S37 AND S12
S39	2	RD (unique items)
S40	1958	S37 NOT S38
S41	15	S40 AND S13
S42	0	S41 AND S16
S43	0	S41 AND S19
S44	15	RD S41 (unique items)
S45	1943	S40 NOT S41
S46	0	S45 AND S13
S47	60	S45 AND S16
S48	0	S47 AND S19
S49	0	S47 AND S22
S50	0	S47 AND S23

S51	0	S47 AND S9
S52	0	S47 AND S10
S53	60	S47 AND S14
S54	0	S53 AND S15
S55	0	S53 AND S17
S56	0	S53 AND S18
S57	0	S53 AND S23
S58	0	S1 AND S12
S59	2751	S8 AND S16
S60	6	S59 AND S19
S61	6	RD (unique items)
S62	2745	S59 NOT S60
S63	123	S62 AND S22
S64	0	S63 AND S23
S65	55	S63 AND S2
S66	55	S65 NOT S44,S41,S30,S34,S26
S67	55	RD (unique items)

27/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

02695208 INSPEC Abstract Number: B86042780
Title: A ceramic-based ozonizer using **high frequency** discharge
Author(s): Masuda, S.; Akutsu, K.; Kuroda, M.; Awatsu, Y.; Shibuya, Y.
Author Affiliation: Dept. of Electr. Eng., Tokyo Univ., Japan
Conference Title: Conference Record. 1985 IEEE Industry Applications Society Annual Meeting (Cat. No.85CH2207-9) p.1353-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1985 Country of Publication: USA xxii+1786 pp.
U.S. Copyright Clearance Center Code: 0090-3507/85/0000-1353$01.00
Conference Sponsor: IEEE
Conference Date: 6-11 Oct. 1985 Conference Location: Toronto, Ont., Canada
Language: English
Abstract: Novel ozonizers have been developed using a ceramic electrostatic functional device as the main component. The device consists of high-purity alumina plates or cylinders comprising tungsten electrodes energized by a **high-frequency**, **high**-voltage power supply.
Two types of ozonizers were built using this device, **one** being a **surface** -discharge type and the other a silent-discharge type. In the former type, the ceramic layer is sandwiched by a **planar induction** electrode and discharge electrode strips, and high voltage is applied between these two electrodes to form an energetic and stable surface discharge. In the latter type, the induction electrode is on one side of the ceramic layer, and the discharge electrode is placed with a small gap, where silent discharge takes place. As both types of ozonizers are produced by well-established ceramic technology in the **IC** and LSI industries, such a device can realize the miniaturization, cost reduction, and high reliability required for small to mid-sized ozonizer applications.
Subfile: B

27/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06767761
MANUFACTURE OF **CHIP** INDUCTOR

PUB. NO.: 2000-353634 [JP 2000353634 A]
PUBLISHED: December 19, 2000 (20001219)
INVENTOR(s): OKAMOTO SHINJI
APPLICANT(s): HOKURIKU ELECTRIC IND CO LTD
APPL. NO.: 11-162717 [JP 99162717]
FILED: June 09, 1999 (19990609)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method for manufacturing a **chip** inductor which is high in production efficiency, easily made small in size and **high** in **inductor performance.**

SOLUTION: A **planar** insulating substrate 12 made of ceramics or having at least its surface of insulating magnetic material is provided, a plurality of rows of openings 14 are formed being spaced by a prescribed interval therebetween, a conductor 20 is formed on the inner surface of each of the openings 14, the conductors 20 are provided at interconnections between the openings 14 in the adjacent rows, and the conductors 20 between the adjacent openings 14 are isolated from each other. The conductors 20 on the front and rear **surfaces** of the **substrate** 12 are electrically connected to each other through the conductors 20 within the openings 14 to form a spiral coil pattern in the substrate 12, the pattern of which is made of the conductors 20 on the front and rear **surfaces** of the **substrate** 12 and made of the conductors 20 within the openings 14, the substrate 12 is divided along the rows of the openings 14 to form **chip** inductors.

30/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

11705698 PASCAL No.: 94-0568766
Planarized thin film **inductors** and capacitors for hybrid **integrated circuits** made of aluminum and anodic alumina
SURGANOV V
Minsk radioeng. inst., res. lab., dep. microelectronics, Minsk 220600, BLR
Journal: IEEE transactions on components, packaging, and manufacturing technology. Part B : Advanced packaging, 1994, 17 (2) 197-200
Language: English
Planarized inductors and capacitors made of aluminum layers by electrochemical anodization technique have been tested in the frequency region of 1 kHz-300 MHz at temperatures of 293-473 K. These microcomponents can be used for **high-frequency** hybrid **integrated circuits**

34/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013506729
WPI Acc No: 2000-678673/200066
XRAM Acc No: C00-206315
XRPX Acc No: N00-502371
Formation of an inductor on a silicon wafer substrate by reverse junctions
Patent Assignee: CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N); CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: SANDFORD CHU S; SHAO K; ZHU M; KAI S; MIN Z; SHAO-FU S C; CHU S S
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6133079	A	20001017	US 99358985	A	19990722	200066	B
EP 1071132	A2	20010124	EP 2000640001	A	20000310	200107	
SG 80666	A1	20010522	SG 996677	A	19991229	200134	
TW 434875	A	20010516	TW 99119087	A	19991102	200170	N

Priority Applications (No Type Date): US 99358985 A 19990722; TW 99119087 A 19991102
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133079	A		10	H01L-021/8238	
EP 1071132	A2	E		H01L-027/06	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
SG 80666	A1			H01L-021/8238	
TW 434875	A			H01L-027/02	

Abstract (Basic): US 6133079 A
Abstract (Basic):
NOVELTY - An inductor is formed on a silicon wafer substrate (20) by reverse p/n junctions between a p-well and the p-type substrate.
DETAILED DESCRIPTION - Formation of an inductor on a silicon wafer substrate comprises providing a silicon wafer of a first conductivity type. A first photoresist layer (21) is patterned to define a first opening (23) in a region (22) of the wafer. A first dose of ions of a second conductivity type is implanted into the first opening at a first energy placing the centroid of the first dose at a first depth below the silicon surface, forming a pocket of the second conductivity type. The **first** photoresist layer is **removed** and the wafer is subjected to a first thermal annealing. A second photoresist layer defining a second opening is patterned wholly within and concentric with the first opening and spaced inward from the perimeter of the first opening by a gap. A second dose of ions of the first conductivity type is implanted at a second energy into the wafer, thus forming a well of the first conductivity type. The second dose is placed at a second depth which is shallower than t he first depth. The **second** photoresist layer is **removed** and the wafer is subjected to a second thermal annealing. Insulative layer(s) is formed over the region. An inductor element is formed on the insulative layers and lying entirely over the well. An INDEPENDENT CLAIM is also included for a method for forming a complementary metal-oxide semiconductor (CMOS) **integrated circuit** with an inductive element.

USE - For forming an inductor on a silicon wafer substrate.

ADVANTAGE - The method reduces inductor-to-substrate capacitance without requiring the application of electrical bias. It improves the **high frequency performance** of an inductor formed in an **integrated circuit**. It forms an inductor element in an **integrated circuit** with low substrate capacitance with low added process complexity.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of a region of a silicon wafer in which an inductor is formed.

Substrate (20)
Photoresist layer (21)
Region (22)
First opening (23)
pp; 10 DwgNo 3A/7

39/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02797025
MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT**

PUB. NO.: 01-094625 [JP 1094625 A]
PUBLISHED: April 13, 1989 (19890413)
INVENTOR(s): HORIBA SHINICHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-252750 [JP 87252750]
FILED: October 06, 1987 (19871006)
JOURNAL: Section: E, Section No. 793, Vol. 13, No. 330, Pg. 76, July 25, 1989 (19890725)

ABSTRACT

PURPOSE: To decrease difference in level of a surface for enabling a resist pattern to be formed thereon exactly according to designed sizes and to provide a semiconductor **integrated circuit** having desirable **performance** with **high** yield at a low price, by forming an insulating film on a **scribing line** region.

CONSTITUTION: A semiconductor **integrated circuit** is manufactured by forming, on a semiconductor substrate 1, a plurality of semiconductor element regions 20 and **scribing line** regions 10 for dividing the regions 20. In this case, an insulating film 4 is formed on said **scribing line** regions 10. For example, following to forming a dopant diffused region or the like in the element **regions** 20 in the **substrate** 1, an insulating film 2 of SiO(sub 2) and a lower interconnection 3 of A are formed. Subsequently an interlayer insulating film 4 of PSG or the like is deposited on the whole surface including the **scribing line** regions 10. An aperture 5 is provided in the interlayer insulating film 4 on the lower interconnection 3, and an A film 6 for providing upper interconnections is formed over the whole surface. A photoresist film 7 for patterning the A film 6 is formed by application technique.

39/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02795520
REDUCED PROJECTION-EXPOSURE DEVICE

PUB. NO.: 01-093120 [JP 1093120 A]
PUBLISHED: April 12, 1989 (19890412)
INVENTOR(s): MATSUKAWA HISAHIRO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-250886 [JP 87250886]
FILED: October 05, 1987 (19871005)
JOURNAL: Section: E, Section No. 792, Vol. 13, No. 325, Pg. 145, July 21, 1989 (19890721)

ABSTRACT

PURPOSE: To conduct a reduced projection-exposure operation with which a pattern can be transferred in a highly precise manner by a method wherein the local inclination of the surface of a wafer is accurately detected without narrowing the width of a laser beam narrower than the width of a **scribe line**.

CONSTITUTION: After a wafer 6 has been moved to the prescribed position by an ordinary positioning mechanism, the inclination of the exposing region such as the wafer **surface** of **one-chip** component is detected by a detecting part 8. Then, at least either of a reticle 4 and a wafer stage is inclined so that the above-mentioned inclination can be corrected. In this case, when the wafer stage only is inclined, the wafer stage is inclined by a stage fine adjust ment part 7 in the amount same as the detected inclination. Also, when the reticle only is inclined, the reticle 4 is inclined five times of the wafer surface detected by the reticle fine adjusting part 5 in the case of 1/5 contraction, for example. Accordingly, a transfer operation can be conducted on the wafer surface in a **highly** precise manner by **performing** the correction of inclination on the exposing region in advance.

44/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015330124
WPI Acc No: 2003-391059/200337
Related WPI Acc No: 2002-290796; 2002-396715; 2002-555993; 2002-573700; 2003-102186; 2003-138414; 2003-310482; 2003-539681
XRAM Acc No: C03-103817
XRPX Acc No: N03-312324

Resistor for **high-performance integrated circuits**, has semiconductor **substrate**, metallization structure, **passivation** layer, openings, resistive layer and conductive layer

Patent Assignee: MEGIC CORP (MEGI-N)
Inventor: LIN M

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6489656	B1	20021203	US 2001970005	A	20011003	200337 B
			US 2002156589	A	20020528	

Priority Applications (No Type Date): US 2001970005 A 20011003; US 2002156589 A 20020528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6489656	B1		20	H01L-023/62	Div ex application US 2001970005 Div ex patent US 6455885

Abstract (Basic): US 6489656 B1
Abstract (Basic):

NOVELTY - A resistor comprises a semiconductor **substrate** (10) containing a **passivation** layer (18) deposited over a metallization structure (14) having electrical contact points. Openings (22, 36, 38) in the passivation layer partially expose pair(s) of contact points that are interconnected by a layer of conductive material. A layer of resistive conducting material is deposited over the passivation layer.

DETAILED DESCRIPTION - The substrate (10) comprises semiconductor devices provided with points of electrical contact. The metallization structure (14) comprises layer(s) of interconnects over **substrate**'s **active surface**. The **interconnect** layers comprise **conductive interconnect** lines (11, 13), **conductive** contact points, or conductive vias within the layers. Points (16) of electrical contact are also provided on the surface of metallization structure, with at least one of the electrical contact points making contact with the **conductive interconnect** lines, contact points, or vias. At least one of the interconnect lines, contact points or conductive vias makes contact with at least one of the electrical contact points provided to the semiconductor devices. At least two of the openings in the passivation layer overlay at least one pair of electrical contact points provided in the metallization structure.

The resistor preferably contains a polymer insulating layer (20) deposited over the surface of patterned and etched passivation layer including the openings. At least one pair of openings in the polymer insulating layer that aligns with at least one pair of openings in the passivation layer, partially exposes at least one pair of electrical contact points provided in the surface of metallization structure.

USE - The resistor is used for **high-performance integrated circuits** (claimed).

ADVANTAGE - The resistor is of high quality.

DESCRIPTION OF DRAWING(S) - The figures show cross-sections of silicon substrate and overlying layers.

Semiconductor substrate (10)
Interconnect lines (11, 13)
Metallization structure (14)
Electrical contact points (16)
Passivation layer (18)
Polymer insulating layer (20)
Openings (22, 36, 38)
pp; 20 DwgNo 4, 10/11

44/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015249556
WPI Acc No: 2003-310482/200330
Related WPI Acc No: 2002-290796; 2002-396715; 2002-555993; 2002-573700; 2003-102186; 2003-138414; 2003-391059; 2003-539681
XRAM Acc No: C03-081263
XRPX Acc No: N03-247034

Capacitor for **high performance integrated circuits** comprises overlaying interconnecting metallization structure, passivation layer, first conductive layer, dielectric layer and second conductive layer

Patent Assignee: MEGIC CORP (MEGI-N)
Inventor: LIN M

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6489647	B1	20021203	US 98216791	A	19981221	200330 B
			US 99251183	A	19990217	
			US 2000721722	A	20001127	
			US 2001970005	A	20011003	
			US 2002156590	A	20020528	

Priority Applications (No Type Date): US 2001970005 A 20011003; US 98216791 A 19981221; US 99251183 A 19990217; US 2000721722 A 20001127; US 2002156590 A 20020528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6489647	B1		20	H01L-027/108	CIP of application US 98216791
					CIP of application US 99251183
					CIP of application US 2000721722
					Div ex application US 2001970005
					CIP of patent US 6303423
					CIP of patent US 6383916
					Div ex patent US 6455885

Abstract (Basic): US 6489647 B1
Abstract (Basic):

NOVELTY - A capacitor comprises a semiconductor substrate (10); an overlaying interconnecting metallization structure (14); a passivation layer (18) deposited over the structure; a first layer of conductive material over passivation layer; a first layer of dielectric over surface of conductive layer; and a second layer of conductive material over dielectric layer surface.

DETAILED DESCRIPTION - A capacitor comprises a dielectric layer (46) interspersed between a top plate (44) and a bottom plate (42) and comprises:

(a) a semiconductor substrate (10), in or on the surface of which semiconductor devices have been created, with points of electrical contact provided to the semiconductor devices in or on the **active surface** of the **substrate**;

(b) an overlaying interconnecting metallization structure (14) comprising layer(s) of interconnects over the active surface of (10), comprising **conductive interconnect** lines, **conductive** contact points or conductive vias in layers, with points of electrical contact provided in or on the surface of (14). At least one of the

points of electrical contact makes contact with the **conductive interconnect** lines, **conductive** contact points or conductive vias provided in the layers of (14). At least one of the metal lines, contact points or conductive vias makes contact with the points of electrical contact provided to the semiconductor devices in or on the surface of (10), the points being divided into pairs of even and odd numbered adjacent contact points. One point of electrical contact can belong to only one pair;

(c) a passivation layer (18) deposited over (14);

(d) openings created in (18). At least one opening overlays at least one even contact point of the points of electrical contact provided in or on the **surface** of (14). A **first** layer of conductive material is deposited over the surface of (18) including the openings;

(e) an opening created in the first layer of conductive material to at least one of the even numbered points of electrical contact provided in or on the **surface** of (14). The **first** layer of conductive material forms the bottom plate of the capacitor. A layer of dielectric (46) is deposited over the **surface** of the **first** layer of conductive material, including the opening to at least one of the even numbered points of electrical contact;

(f) an opening in (46) to at least one of the even numbered points of electrical contact, partially exposes at least one of the even numbered points of electrical contact and forms the layer of dielectric interspersed between the top and bottom plates;

(g) a second layer of conductive material deposited over the surface of (46), including at least one opening created in (46); and

(h) creating the top plate of the capacitor (44) by patterning and etching the second layer of conductive material.

USE - The capacitor is used for **high performance integrated circuits** (claimed).

ADVANTAGE - The invention provides **high performance** electrical components on the **surface** of a semiconductor **substrate** by reducing the electromagnetic losses typically incurred in the **surface** of the **substrate.**

DESCRIPTION OF DRAWING(S) - The figure shows cross-sections of a substrate and overlaying layers.

Substrate (10)
Layer of interconnect (14)
Passivation layer (18)
Bottom plate (42)
Top plate (44)
Layer of dielectric (46)
pp; 20 DwgNo 4, 6a/11

44/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015209416
WPI Acc No: 2003-269952/200327
XRAM Acc No: C03-070989
XRPX Acc No: N03-214186
Molded **chip** scale package semiconductor device for small area semiconductor **chip**, has bumped **integrated circuit chip**, flexible film interposer, underfill material, molded epoxy encapsulation and external solder ball connectors
Patent Assignee: TEXAS INSTR INC (TEXI); COYLE A L (COYL-I)
Inventor: COLYE A L; COYLE A L
Number of Countries: 028 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1229577	A2	20020807	EP 2002100086	A	20020130	200327 B
JP 2002252303	A	20020906	JP 200225401	A	20020201	200327
US 20020105092	A1	20020808	US 2001776465	A	20010202	200327
US 6518089	B2	20030211	US 2001776465	A	20010202	200327
US 20030092217	A1	20030515	US 2001776465	A	20010202	200335
			US 2002320585	A	20021216	

Priority Applications (No Type Date): US 2001776465 A 20010202; US 2002320585 A 20021216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1229577	A2	E	9	H01L-021/56	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002252303	A		8	H01L-023/12	
US 20020105092	A1			H01L-023/48	
US 6518089	B2			H01L-021/44	
US 20030092217	A1			H01L-021/44	Div ex application US 2001776465 Div ex patent US 6518089

Abstract (Basic): EP 1229577 A2
Abstract (Basic):
NOVELTY - A molded **chip** scale package (CSP) semiconductor device comprises a bumped **integrated circuit chip** (30) positioned as a flip **chip**, a flexible film interposer, an underfill material (34), a molded epoxy encapsulation and external solder ball (37) connectors.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for assembling multiple plastic molded flip **chip** packaged semiconductor devices having low inductance interconnections comprising:
(a) aligning and attaching a semiconductor **chips** having bump contacts to a strip of flexible tape interposer;
(b) applying a polymeric underfill material between each **chip** and interposer, and partially curing the polymer;
(c) injecting a molding compound (38) to fill one or cavities in a mold die where the **chips** connected to an interposer are positioned, and curing the molding and underfill compounds;
(d) attaching a solder balls to the terminals of the vias on

second surface (321) of the interposer; and
(e) singulating the assemblage into individual devices.
The interposer is a dielectric tape having lands corresponding to **chip** bump contacts and **conductive interconnections** patterned on the **first** major **surface** and routed to vias extending through the tape to the **second surface**.
USE - Small area semiconductor **chip**.
ADVANTAGE - Provides a **high performance, high** speed, low inductance package. It is compatible with required reliability standards of small area **integrated circuits**.
DESCRIPTION OF DRAWING(S) - The figure is a cross-section of an CSP.
Bumped **integrated circuit chip** (30)
Underfill material (34)
Solder ball (37)
Molding compound (38)
Second surface (321)
pp; 9 DwgNo 3/6

44/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014860449
WPI Acc No: 2002-681155/200273
XRAM Acc No: C02-192165
XRPX Acc No: N02-537632
Multiple layer inductor for **integrated circuits**, comprises substrate, first patterned conductor layer, layer of insulating material, and second patterned conductor layer
Patent Assignee: TYCO ELECTRONICS CORP (TYCO-N)
Inventor: BEAUSSART S; STRUBLE W M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6429504	B1	20020806	US 2000571909	A	20000516	200273	B

Priority Applications (No Type Date): US 2000571909 A 20000516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6429504	B1		9	H01L-029/00	

Abstract (Basic): US 6429504 B1
Abstract (Basic):
NOVELTY - A multiple layer inductor comprises a substrate of semiconductor material; a first patterned conductor layer; a layer of insulating material over the first patterned conductor layer; and a second patterned conductor layer. The first patterned conductor layer is formed on a **surface** of the **substrate**, while the second is formed on a surface of the layer of insulating material.

DETAILED DESCRIPTION - A multiple layer inductor comprises:

(a) a substrate (106) of semiconductor material;

(b) a first patterned conductor layer (102);

(c) a layer of insulating material over the first patterned conductor layer; and

(d) a second patterned conductor layer (104) having a pre-designed geometric shape.

The first patterned conductor layer is formed on a **surface** of the **substrate**, while the second is formed on a surface of the layer of insulating material. The first and second patterned conductor layers comprise a first loop (102a, 102b, 102c, 104a, 104b, 104c) defining a first end and a second end. The first and second patterned conductor layers are dimensioned and arranged to provide a first and a second portion, respectively, of a desired inductance value. The first end of the first loop of the first patterned **conductor** layer is **interconnected** to a first end of the first loop of the second patterned conductor layer by a conductive link that extends through the layer of insulating material. The first and/or the second patterned conductor layer further includes a second loop having a first end and a second end, and is dimensioned to provide a third portion of a desired inductance value. A first end of the second loop is interconnected to a second end of one of the first loops by a conductive link extending through the layer of insulating material.

An INDEPENDENT CLAIM is included for a microwave **integrated circuit** comprising:

(i) a substrate of semiconductor material comprising a first

patterned conductor layer;
(ii) a layer of insulating material on the first patterned conductor layer, having a second patterned conductor layer on it; and
(iii) an active device.
USE - For **integrated circuits**.
ADVANTAGE - The conductor has an arrangement that is more compact. It operates at a much **higher frequency** than that practically possible before.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a multi-layer inductor structure.
First patterned conductor layer (102)
Second patterned conductor layer (104)
Substrate (106)
First loop (102a, 102b, 102c, 104a, 104b, 104c)
pp; 9 DwgNo 3/5

44/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014596348
WPI Acc No: 2002-417052/200244
XRAM Acc No: C02-117674
XRPX Acc No: N02-328203
Fabrication of heterojunction photodiode monolithically integrated with complementary oxide semiconductor involves selective epitaxial growth of photodiode module on selected active areas
Patent Assignee: AUGUSTO C J R P (AUGU-I); FORESTER L (FORE-I)
Inventor: AUGUSTO C J R P; FORESTER L
Number of Countries: 097 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200233755	A2	20020425	WO 2001EP11817	A	20011012	200244	B
AU 200195618	A	20020429	AU 200195618	A	20011012	200255	
EP 1328975	A2	20030723	EP 2001976306	A	20011012	200350	
			WO 2001EP11817	A	20011012		

Priority Applications (No Type Date): US 2000241551 P 20001019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200233755	A2	E	55	H01L-027/144	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200195618	A		H01L-027/144	Based on patent WO 200233755
EP 1328975	A2	E	H01L-027/144	Based on patent WO 200233755

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200233755 A2
Abstract (Basic):
NOVELTY - Fabricating a heterojunction photodiode monolithically integrated with complementary oxide semiconductor (CMOS) comprises selective epitaxial growth of a photodiode module on selected active areas of CMOS structures; formation of contact layer for metal interconnects on at least the selected areas; and formation of metal interconnects on top of the contact layer.
DETAILED DESCRIPTION - Fabricating a heterojunction photodiode monolithically integrated with a complementary metal oxide semiconductor (CMOS) comprises fabrication of CMOS structures having active areas on a semiconductor substrate with standard CMOS processing and/or implanting only one doping type for both well and junction. A photodiode module is selectively epitaxially grown on selected active areas. A contact layer is formed for metal interconnects on at least the selected areas of each epitaxially grown photodiode module. Metal interconnects are formed on top of the contact layer.
INDEPENDENT CLAIMS are included for the following:
(a) A CMOS imager sensor including a common semiconductor substrate and side-by-side spaced apart integrated light-sensing devices for

sensing a specific range of wavelengths in the visible, infra-red and/or ultra-violet spectrum; and

(b) An optical electronic transceiver comprising CMOS **circuitry** monolithically **integrated** with light-sensing devices.

USE - For fabricating a heterojunction photodiode monolithically integrated with CMOS.

ADVANTAGE - Since the **active region** is epitaxially deposited, sharp doping profiles and band-gap engineering are formed during the epitaxial process to optimize several device parameters for **higher performance**. This new type of light sensor architecture, monolithically integrated with CMOS, decouples the photo-absorption **active region** from the metal oxide semiconductor field effect transistors (MOSFETs). The bias applied to the photodiode can be independent from the bias between the source, drain, gate and substrate (well) of the MOSFETs.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a photodiode module of the invention.

pp; 55 DwgNo 2/11

44/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014403682
WPI Acc No: 2002-224385/200228
Related WPI Acc No: 2003-567006
XRPX Acc No: N02-171850
Microelectronic package fabrication and method, comprises a thin film decal and a dielectric adhesive layer that includes a number of conductive vias between two microelectronic substrates
Patent Assignee: VIRTUAL INTEGRATION INC (VIRT-N)
Inventor: JACOBS S L; JACOBS S
Number of Countries: 097 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6294407	B1	20010925	US 9884450	P	19980506	200228	B
			US 99306463	A	19990505		
WO 200317367	A1	20030227	WO 2001IB1487	A	20010817	200316	N

Priority Applications (No Type Date): US 9884450 P 19980506; US 99306463 A 19990505; WO 2001IB1487 A 20010817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6294407	B1		23	H01L-021/44	Provisional application US 9884450
WO 200317367	A1	E		H01L-023/498	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

Abstract (Basic): US 6294407 B1
Abstract (Basic):

NOVELTY - Microelectronic package (100) fabrication method comprising the formation of a release layer on a process substrate e.g. glass silicon or other sacrificial substrates. A thin film decal (110) formed on the release layer. The thin film decal has two opposing decal faces, a quantity of decal input/output pads (112) on the first decal face, and a quantity of second decal input/output pads (122) on the second decal face.

DETAILED DESCRIPTION - At least one internal wiring layer is electrically connected to at least one of the first and second decal input/output pads. The first decal input/output pads are adjacent the release layer and the second decal input/output pads are remote from the release layer.

A dielectric adhesive layer (130) is formed on the second decal face two opposing faces and a quantity of conductive vias (132) that extend between the two layer faces. The first dielectric adhesive layer face is adjacent the second decal face and the second adhesive dielectric layer face is remote from the second decal face, such that at least one of the conductive vias electrically connects to at least one of the second decal input/output pads.

The second face of the dielectric adhesive layer is adhesive bonded to a second level substrate with a quantity of second level substrate

input/output pads on a face, such that the conductive vias electrically connect the second level substrate input/output pads.

The release layer is etched in a batch process to release the substrate from on the first face of the thin film decal, which is then followed by bonding a first level substrate. This includes a plurality of microelectronic devices and a plurality of first level substrate input/output pads on a face thereof to the first decal face layer such that at least one of the conductive vias electrically connects to at least one of the first level substrate input/output pads.

The dielectric adhesive layer with a quantity of holes is formed on the second decal face by adhesive bonding to the second decal face such that it laterally overlaps at least one of the second decal input/output pads. Conductive adhesive is then screened into the holes in the dielectric adhesive layer. The release layer is processed by dissolving in an etch batch process.

The first level substrate may be a flip-**chip** or other **integrated circuit** and/or other first level microelectronic and the second level substrate is a printed circuit board.

The first level substrate bonding involves the step of re-flowing solder bumps between the first level substrate input/output pads and the first decal face.

Lithography is used to create the thin film decal with a rippled **first surface** and rippled internal wiring layer.

The processing of the release layer to release the substrate from the first face of the thin film decal includes the use of a laser to destroy bonds between the thin film decal and the substrate.

The thin film decal and dielectric adhesive layer with conductive vias, that can be used between a first level substrate and a second level substrate, is regarded as a Planar Graft Patch (PGP)

USE - To provide;

(1) Improved microelectronic packages and methods of fabrication.

(2) Microelectronic packages than can allow high density wiring to be used with conventional printed circuit boards.

(3) Microelectronic packaging an fabrication methods that can allow conventional printed circuit technology to be extended to **high performance** and/or **high** density microelectronic systems.

ADVANTAGE - The combination of the thin film decal and the dielectric adhesive layer including a number of **conductive** vias provides an **interconnect** packaging technology that can be low cost and/or high density, and can be produced by standard board process technology, thus extending the capabilities of printed circuit board technology.

DESCRIPTION OF DRAWING(S) - The drawing figure 1 shows a cross sectional view of the microelectronic package.

Microelectronic package (100)

thin film decal (110)

decal input/output pads (112, 122)

dielectric adhesive layer (130)

conductive vias (132)

pp; 23 DwgNo 1/13

44/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013177755
WPI Acc No: 2000-349628/200030
XRAM Acc No: C00-106301
XRPX Acc No: N00-261940
Controlled test alignment fixture for **integrated circuit** package testing operation utilizes gold contacts on a high dielectric test substrate in combination with a thin conductive material
Patent Assignee: LUCENT TECHNOLOGIES INC (LUCE)
Inventor: CRISPELL R B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6057700	A	20000502	US 9873279	A	19980506	200030	B

Priority Applications (No Type Date): US 9873279 A 19980506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057700	A		6	G01R-031/02	

Abstract (Basic): US 6057700 A
Abstract (Basic):

NOVELTY - An alignment fixture utilizes gold contacts on a high dielectric test substrate in combination with a thin pressure-induced conductive material, so as to have a **high** speed capability in **performance** testing.

DETAILED DESCRIPTION - An alignment fixture (10) for performing tests on an **integrated circuit** package (26) comprises (a) a test substrate (12) including test leads (28) formed on its surface; (b) a pressure-induced conductive material (14) disposed to cover the test leads; (c) a fixture base (18) unit including alignment fiducials (20, 22); (d) a fixture lid (30) unit formed to mate with the base unit and comprising vertically oriented tab portions (34) that extend into the base unit aperture upon mating. An INDEPENDENT CLAIM is also included for a method of testing an **integrated circuit** package comprising (a) providing a test substrate including test leads formed on its surface; (b) placing a layer of pressure-induced conductive material on the test substrate so as to cover the test leads; (c) attaching a fixture base unit having alignment fiducials to the test substrate so as to engage the alignment fiducials; (d) inserting an **integrated circuit** package into the base unit so that external leads of the package rest upon layer of pressure-induced conductive material; (e) placing a fixture lid unit over the base unit in which the lid unit comprises vertically oriented tab portions that extend downward into the base unit aperture and contact the exposed leads of the **integrated circuit** package; (f) applying a predetermined force to the fixture lid unit so as to force the tabs onto the package leads and induce conductivity within the pressure-induced conductive material, thus forming a conductive path between the substrate test leads and the **integrated circuit** package leads; and (g) testing the electric performance of the **integrated circuit** package.

USE - For implementing radio frequency (RF) and direct current (DC) testing of **integrated circuit** packages.

ADVANTAGE - The invention is capable of **performing high** speed **performance** testing and of performing repeatable testing processes on large volumes of **integrated circuit** packages.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded view of the pressured controlled test fixture.

Alignment fixture (10)
Test substrate (12)
Conductive material (14)
Fixture base (18)
Fiducials (20, 22)
Package (26)
Test leads (28)
Fixture lid (30)
Tab portions (34)
pp; 6 DwgNo 1/3

44/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012325206
WPI Acc No: 1999-131313/199911
XRAM Acc No: C99-038299
XRPX Acc No: N99-095656
Multi-level transistor fabrication - comprises forming an inverted upper level transistor above another transistor with ohmic contact at silicide between the two gate conductors of the two transistors
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: GARNDER M I; KADOSH D; PAIZ R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5863818	A	19990126	US 96727050	A	19961008	199911	B

Priority Applications (No Type Date): US 96727050 A 19961008
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5863818	A		10	H01L-021/00	

Abstract (Basic): US 5863818 A

Interconnecting a first gate **conductor** of a first transistor (14) to a second gate conductor of a second transistor (52), comprises: (a) forming a silicide (30) upon the first gate conductor (20); (b) depositing an interlevel dielectric (32) across the silicide; (c) forming an opening through the interlevel dielectric to the silicide; (d) filling the opening with a second gate conductor (40); (e) growing a gate dielectric on the second gate conductor; (f) depositing a substrate (44) on the gate dielectric; (g) patterning the substrate; (h) implanting source and drain **regions** (50) into the **substrate** to form a second transistor (52) with a second gate conductor at an elevation level below the gate dielectric and the source and drain regions.

USE - Multi-level transistor fabrication with **high performance** interconnect.

ADVANTAGE - The process can produce p-type and/or n-type devices in three dimensions to enhance the overall density at which an **IC** is formed. Gate conductor of second transistor is doped opposite gate conductor of first transistor. This ensures an ohmic contact at silicide, ensuring that both polysilicon gates will be at the same bias, a desired outcome in circuit applications. A **high performance** interconnect is achieved.

Dwg.9/10

44/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009881247
WPI Acc No: 1994-161161/199420
Related WPI Acc No: 1993-086850
XRAM Acc No: C94-073740
XRPX Acc No: N94-126818
Carbon fluoride-contg. polymer composite material for electronic circuit - obtd. by dispersing fluorinated granular carbon@ into polymer of specified dielectric constant
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: AFZALI-ARDAKANI A; AYALA-ESQUILIN J; BRAREN B E; DAIJAVAD S; FOSTER E; HEDRICK J C; HEDRICK J L; HODGSON R T; MEHTA A A; MOLIS S E; SHAW J M; TISDALE S L; VIEHBECK A
Number of Countries: 002 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6061597	A	19940304	JP 92241572	A	19920910	199420	B
US 5397863	A	19950314	US 91759377	A	19910913	199516	
			US 91759380	A	19910913		
			US 92929313	A	19920813		
JP 95073151	B2	19950802	JP 92241572	A	19920910	199535	
US 5556899	A	19960917	US 91759377	A	19910913	199643	
			US 91759380	A	19910913		

Priority Applications (No Type Date): US 92929313 A 19920813; US 91759377 A 19910913; US 91759380 A 19910913; US 94346766 A 19941130; US 95472120 A 19950607; US 95475670 A 19950724
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6061597	A		13	H05K-001/03	
US 5397863	A		10	H05K-001/03	CIP of application US 91759377
					CIP of application US 91759380

Abstract (Basic): JP 6061597 A
A fluorinated granular carbon material is dispersed into a polymer material having dielectric constant to form a composite material. The composite material has lower dielectric constant than that of the polymer material. The carbon fluoride-contg. polymer composite material contains the composite material, and a conductor pattern-provided substrate.
Pref. the polymer material comprises: an epoxy resin, polycyanurate, polysiloxane, polybenzocyclobutene, bismaleimide polymer, or polyquinoxaline.
USE/ADVANTAGE - The carbon fluoride-contg. polymer composite material is used for producing electronic **circuits**, including **integrated circuits**, printed **circuits**, or circuit substrates. The composite material changes the physical properties of the polymer material (Reissue of the entry advised in week 9414 based on complete specification).
Dwg.0/0
Abstract (Equivalent): US 5591285 A
A method for making a dielectric material of a fluoropolymer and **fluorinated carbon** comprising the steps of: mixing a supply

of fluorinated carbon particles in a supply of fluoropolymer with the fluorinated carbon to fluoropolymer being in the range of 2% to 60% by wt., and where the fluorinated carbon particles contain from 28 to 64 atomic wt. percent of fluorine; treating the mixt. to form a composite of it; laminating the composite at a pressure in the range from about 100-200 psi and at a temp. in the range from 350deg.C to 390deg.C.; and exposing an area of the laminated composite to UV excimer laser radiation at a fluence in the range from 50 to 1000 mJ/cm2 to partially defluorinate the fluorinated carbon and render the exposed area of the composite electrically **conductive**.

Dwg.0/0

US 5571852 A

A process of forming a polymeric composite material with at least **one surface** conductive region in the polymeric composite material contg. a fluorinated carbon material comprising irradiating the polymeric composite material with a pulsed UV laser where the polymeric material is selected from the gp. consisting of polyimides, fluoropolymers, epoxies, polycyanurates, polysiloxanes, polybenzocyclobutenes, polyquinoxalines and bismaleimides and where the fluorinated carbon material contains 28-75 atomic wt.% of fluorine.

Dwg.0/0

US 5556899 A

A process of effecting a change of the physical properties of a polyimide material, where the properties are dielectric constant and reduced coefficient of thermal expansion, comprising forming a polyimide composite material having a low dielectric constant, said composite based on a dispersion consisting of a fluorinated particulate carbon material and a polyimide or polyimide precursor and optionally one or both of a liquid solvent and a liquid carrier and optionally a coupling agent, said fluorinated carbon material being present in an amount of 2-60 %wt. and heating the dispersion to 400 deg.C at a rate of 65-220 deg.C per second.

Dwg.0/0

US 5397863 A

A structure comprises a substrate formed from a dielectric material comprising a composite of fluorinated particulate C material dispersed in a polymeric material having a dielectric constant. The C material contains 28-75 atomic wt.% F. The C material is contained in an amt. to give the composite a dielectric constant less than the dielectric constant of the polymeric material. The substrate includes electrical conductor patterns.

Pref., the polymeric material comprises e.g. polyimide, fluoropolymer or bismaleimide, etc. The structure also includes an electronic device which is electronically **interconnected** with the **conductor** patterns.

USE - Used for forming **high performance** electronic device packaging and PCB's.

Dwg.0/0

44/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009840379
WPI Acc No: 1994-120235/199415
XRPX Acc No: N94-094184
Multichip module **IC** device having max input-output capability - has array of functional circuits whose inputs and outputs are interconnected via programmable interconnect architecture having two types of drive nodes
Patent Assignee: APTIX CORP (APTI-N)
Inventor: MOHSEN A
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 592111	A2	19940413	EP 93307118	A	19930909	199415	B
JP 7007128	A	19950110	JP 93277459	A	19931008	199511	
US 5432708	A	19950711	US 92958872	A	19921008	199533	
EP 592111	A3	19941221				199537	

Priority Applications (No Type Date): US 92958872 A 19921008
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 592111	A2	E	10	H01L-023/522	
Designated States (Regional): DE FR GB IT					
JP 7007128	A		8	H01L-023/538	
US 5432708	A		9	H03K-017/693	
EP 592111	A3			H01L-023/522	

Abstract (Basic): EP 592111 A

The **integrated circuit** device (10) includes an array of functional circuits (12a-12d) each of which includes a number of inputs (14a,16a,18a,20a) and at least one output (22a,24a) capable of driving a relatively small load. A programmable **interconnect** architecture comprising **interconnect conductors** is superimposed on the functional circuit array.

Direct connections to inputs and outputs of the functional circuits is provided via access **conductors** associated with the **interconnect** structure and which have two different types of input-output nodes. One type of node has a high current drive capability for driving off-**chip** signals with large load capacitances, and one has a low current drive capability.

USE/ADVANTAGE - Form very high I/O density **integrated circuit** for MCM substrate. Has I/O capability of about 10 times that of current devices enabling building programmable device having 100,000 gates more economically and at **higher performance**.

Dwg.1/4

Abstract (Equivalent): US 5432708 A

The high I/O count **integrated circuit** is positioned on a semiconductor die having opposite faces and includes a number of functional circuit modules, each having inputs and an output. A number of I/O nodes, each including a conductive structure, are located in a I/O node array on the **substrate surface**. A number of a second type of I/O nodes, each comprising a first conductive structure is disposed on the first semiconductor **chip** face.

An interconnect architecture comprising a number of conductors is superimposed on the functional circuit modules, the interconnect architecture comprises a number of **interconnect conductors**. Selected **interconnect conductors** are connectable to the inputs and at least one output of selected ones of the functional circuit modules by electrically programmable user-programmable **interconnect** elements. Selected **interconnect conductors** are connectable to other selected **interconnect conductors** by user-programmable **interconnect** elements. Selected **interconnect conductors** are connectable to the first I/O nodes by electrically programmable user-programmable **interconnect** elements. Selected **interconnect conductors** are connectable to the second I/O nodes by electrically programmable user-programmable interconnect elements.

USE - Reprogrammable ASICs with gate counts over 10000, up to 100000.

Dwg.1/4

44/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009048032
WPI Acc No: 1992-175403/199221
XRAM Acc No: C92-080521
XRPX Acc No: N92-132235
Multi-**chip** module system - comprises stacked packages having surface contact pads connected internally and encapsulated **integrated circuit chips**
Patent Assignee: INTEGRATED SYSTEMS ASSEMBLIES CORP (INTE-N); INTEGRATED SYSTEM ASSEMBLIES CORP (INTE-N); EICHELBERGER C W (EICH-I)
Inventor: EICHELBERGER C W
Number of Countries: 020 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5111278	A	19920505	US 91676936	A	19910327	199221	B
WO 9217903	A2	19921015	WO 92US2479	A	19920326	199244	
AU 9217678	A	19921102	AU 9217678	A	19920326	199305	
			WO 92US2479	A	19920326		

Priority Applications (No Type Date): US 91676936 A 19910327
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5111278	A		30		
WO 9217903	A2	E	94	H01L-023/16	
Designated States (National): AU CA JP KR					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU MC NL SE					
AU 9217678	A			H01L-023/16	Based on patent WO 9217903
EP 577754	A1	E		H01L-023/16	Based on patent WO 9217903

Abstract (Basic): US 5111278 A
Multi-**chip** **integrated circuit** package (20) comprises **integrated circuit chips** (38) disposed on the upper **surface** (33) of a **substrate** (30), each having at least one interconnection pad on its top surface, and encapsulant (42) surrounding the **chips** having via openings aligned with at least some of the interconnection pads. A pattern of **interconnection conductors** (46) above the encapsulant extends between at least some of the openings and provides electrical connection to at least some of the pads through the openings and conductive means (43) disposed within the substrate and the encapsulant provides electrical connection between the lower **surface** of the **substrate** and the **interconnection conductors** above the encapsulant, the conductive means passing between the **chips** in the encapsulant.
USE/ADVANTAGE - Package provides a multi-**chip** module in highly planar structure having enhanced resolution, reduced interference to the next level and heat sink, and stacking capability. It can operate at **high frequency**, the impedance of the interconnections being matched, the interconnections shielded, and short connections being provided between all components. The module can be tested before assembly and a module can be removed from a stack and replaced easily. (2/18)
Dwg.2/18

44/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008689404
WPI Acc No: 1991-193424/199126
XRPX Acc No: N91-148085
IC high power, high density interconnection - has multilayer circuit boards comprised of substrates with different interconnect densities
Patent Assignee: CRAY RES INC (CRAY)
Inventor: AUGUST M C; KRUCHOWSKI J N; SHEPHERD L T; AUGUST M
Number of Countries: 016 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9108588	A	19910613				199126 B
US 5127986	A	19920707	US 89444747	A	19891201	199230
US 5185502	A	19930209	US 89444747	A	19891201	199308
			US 90598103	A	19901016	

Priority Applications (No Type Date): US 89444747 A 19891201; US 90598103 A 19901016
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9108588	A				
Designated States (National): CA JP KR					
Designated States (Regional): AT BE CH DE DK ES FR GB IT LU NL SE					
US 5127986	A		9	B44C-001/22	
US 5185502	A		9	H05K-001/00	Div ex application US 89444747

Abstract (Basic): WO 9108588 A
The interconnection module comprises a substrate power bus having voltage and ground vias, with power planes and ground planes sandwiched by dielectric and selectively connected to via. An interconnect substrate mechanically and electrically connected to the substrate power bus, having voltage, ground and signal vias selectively connected to the substrate power bus, and comprises power, ground and signal planes sandwiched by dielectric and selectively connected to the vias.
The interconnect substrate is built-up using **integrated circuit** technology, printed **circuit** board technology and heavy-build electroless plating, with foils comprising planes being thicker than thin film foils.
USE/ADVANTAGE - Improved method for manufacturing circuit boards with high power, high density interconnects minimises DC voltage drops so conductors can run for longer distances, provides conductors with better **performance** for **high frequency** signals and enhances power distribution capabilities. (20pp Dwg.No.8/8)
Abstract (Equivalent): US 5185502 A
The multilayer circuit board includes a substrate power bus layer with an interconnect density having a number of substrate copper layers interleaved with a number of dielectric layers. The substrate copper and dielectric layers form a distribution network of ground voltage and electrical power at different voltage levels using selectively placed vias to distribute the ground voltages and electrical power to each of **two** major **surfaces** of the **substrate** power bus layer.

At least one low density interconnect substrate has a second interconnect density which is higher than the first interconnect density. Each low density interconnect substrate is mechanically and electrically connected to each major **surface** of the **substrate** power bus layer and distributes electrical signals, ground voltage and electrical power at different voltage levels using selectively placed vias interconnecting a number of low density copper layers interleaved with a number of dielectric layers.

At least one high density interconnect substrate has a third interconnect density which is higher than the second interconnect density. Each high density interconnect substrate is mechanically and electrically connected to each low density interconnect substrate, further distributing electrical signals, ground voltage and electrical power at different voltage levels using selectively placed vias **interconnecting** a number of **conductive** layers interleaved with a number of dielectric layers. Each high density substrate further has means for attaching **integrated circuit** die to the high density substrate.

ADVANTAGE - Enhanced power distribution capabilities.

Thicker foils minimise DC voltage drops, so that conductors can run for longer distances. Better HF signal performance.

Dwg.4B/8

US 5127986 A

Printed **circuit** board technology, **integrated circuit** technology, and heavy-build electroless plating are combined to produce multilayer circuit boards comprised of substrates with different interconnect densities. In the higher density substrates, thick metalised layers are built-up by combining additive and subtractive technique. These thicker foils minimise DC voltage drop so that conductors can run for longer distance.

The conductors are more square than their thin film equivalents, thus providing better **performance** for **high frequency** signals. Power distribution capabilities are enhanced so that circuit boards fully populated with dense, high-speed, high-power **integrated circuits** can easily be supplied with their necessary power requirements.

USE/ADVANTAGE - Improved method for manufacturing circuit boards with high power, high density interconnects.

Dwg. 8/8

44/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007797568
WPI Acc No: 1989-062680/198909
XRPX Acc No: N89-047831
Integrated semiconductor **circuit** with decoupled DC wiring - has thinner section of insulating layer located above highly doped surface zone in semiconductor region
Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG)
Inventor: GRIFT R E J; LINSSEN A; VEEN M
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 305001	A	19890301	EP 88201774	A	19880818	198909	B
NL 8701997	A	19890316				198915	
JP 1069034	A	19890315	JP 88207478	A	19880823	198917	
US 5008731	A	19910416	US 90483290	A	19900216	199118	

Priority Applications (No Type Date): NL 871997 A 19870826
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 305001	A	E	7		

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 305001 A

The circuit has a semiconductor region adjoining a surface of a semiconductor body and covered with an electrically insulating layer. The semiconductor region has a number of semiconductor circuit elements **interconnected** by **conductor** tracks disposed on the insulating layer and constituting the wiring of the circuit. A part of the wiring is only intended to contain D.C. information and constitutes the D.C. wiring. The insulating layer under part of the D.C. wiring is considerably thinner than under the wiring parts not formed of D.C. wiring. This thinner part is located on a part of the semiconductor surface which is connected to a connection conductor.

The thinner part of the insulating layer is located above a highly doped surface zone in the semiconductor region. This connects one opening in the insulating layer to the connection conductor.

USE/ADVANTAGE - To reduce **high frequency** interference without additional semiconductor surface area being required.

2/7

Abstract (Equivalent): US 5008731 A

The monolithic **integrated** semiconductor **circuit** has a semiconductor region adjoining a surface of a semiconductor body and covered with an electrically insulating layer. The semiconductor region includes semiconductor circuit elements **interconnected** by **conductor** tracks disposed on the insulating layer and comprising the wiring of the circuit. The wiring includes appts. for carrying only D.C. information and comprising a conductor track. The wiring includes appts. for carrying A.C. information and comprising second conductor track.

The insulating layer has a layer portion under only the second conductor track and a second thinner adjacent layer portion under only the first conductor track and located alongside the first layer

portion. The conductor tracks are on different levels. A connection conductor is connected to a part of the semiconductor **surface**. The **second** layer portion is located on the part of the semiconductor surface which is connected to the connection conductor.

ADVANTAGE - Reduces HF interference. (4pp

44/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004484959
WPI Acc No: 1985-311837/198550
XRAM Acc No: C85-134596
XRPX Acc No: N85-231534
Structure and method for reducing signal losses in VLSI circuits - includes mutually insulated ground plate and conductive signal layers overlying **active** device **region**
Patent Assignee: FAIRCHILD CAMERA CORP (FAIH)
Inventor: EARLY J M
Number of Countries: 007 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 163795	A	19851211				198550	B
JP 60198753	A	19851008	JP 84260105	A	19841211	198601	
US 4833521	A	19890523	US 88218433	A	19880708	198924	

Priority Applications (No Type Date): US 83561017 A 19831213; US 86894452 A 19860804; US 87117454 A 19871102
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 163795	A	E	22		

Designated States (Regional): DE FR GB IT NL

Abstract (Basic): EP 163795 A

Semiconductor structure includes, in sequence: a semiconductor layer contg. active devices; a first dielectric layer; a conductive ground plane (or at least one conductive signal path); a second dielectric layer; and at least one conductive signal path (or a conductive ground plane). First and second dielectric layers are pref. SiO2 or Si3N4; conductive layers are pref. of Al(alloy) or poly-Si.

USE/ADVANTAGE - In VLSI circuits operating at very **high frequencies** or pulse rates. Device provides low combined series resistance thus minimising signal attenuation.

2a/5

Abstract (Equivalent): US 4833521 A

Semiconductor structure comprises: (a) a layer of semiconductor material having **active regions** formed in it; b) a first **conductive interconnecting** signal layer; c) a first conductive ground plane layer disposed between b) and the semiconductor material; d) a second conductive ground plane layer; e) a second **conductive interconnecting** signal layer disposed between b) and d); and f) several dielectric layers for electrically insulating c) and d), b) and e) and the semiconductor material from each other, each of the layers being provided with a means for permitting an electrical connection from any of the conductive layers located above one of the said layers to selected regions of the semiconductor material.

The first and second ground planes are sufficiently continuous and sufficiently conductive to adequately reduce coupling between the conductive signal path and the semiconductor material. The first and second conductive ground planes have several connections with one or more of the active devices.

The first and second conductive ground planes, and at least one conductive signal path, serves as a transmission line of predetermined

characteristic impedance.

ADVANTAGE - An **integrated circuit** is provided having a relatively low combined series resistance to **high frequency** signals.

44/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004099513
WPI Acc No: 1984-245054/198440
XRPX Acc No: N84-183318
High density LSI logic circuit package alumina ceramic substrate - has input and output pins on under surface and multiple wiring layers on upper surface overlaid by leadless **chip** carriers
Patent Assignee: NEC CORP (NIDE)
Inventor: UMETA J; WATARI T
Number of Countries: 007 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 120500	A	19841003	EP 84103423	A	19840328	198440	B
JP 59178759	A	19841011	JP 8352944	A	19830329	198447	
JP 59198737	A	19841110	JP 8373293	A	19830426	198451	
JP 59198738	A	19841110	JP 8373294	A	19830426	198451	
US 4652970	A	19870324	US 85758951	A	19850725	198714	
CA 1229155	A	19871110				198749	
US 4744007	A	19880510	US 86896348	A	19860814	198821	
EP 120500	B	19890816				198933	
DE 3479463	G	19890921				198939	

Priority Applications (No Type Date): JP 8373294 A 19830426; JP 8352944 A 19830329; JP 8373293 A 19830426
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 120500	A	E	32		
Designated States (Regional): DE FR GB NL					
EP 120500	B	E			
Designated States (Regional): DE FR GB NL					

Abstract (Basic): EP 120500 A

The substrate contains a power supply wiring layer, a ground wiring layer and through-hole wires. The latter connect input/output pins on the under surface to multiple wiring layers on the top surface. The multiple wiring layers comprise a first layer having thin-film conductive wiring formed over an insulating film. The insulating film is made of organic high polymer.

Several via-holes connect the first layer to the through-holes wires of the layer underneath. Similarly, a second thin film conductive wiring is formed over an insulating film. A number of leadless **chip** carriers are arranged over the upper surface of the multiple wiring layers. The latter connect a terminal of any carrier to any other terminal and to any input and output pins.

ADVANTAGE - Has high-speed and **high**-density **performance** nad has excellent heat-diffusing properties by mounting **chip** carriers face-down.

0/12

Abstract (Equivalent): EP 120500 B

A multi-**chip** package comprising: an alumina ceramic substrate (1) having, on its under surface, a plurality of input and output pins (11) erected in a grid form and, inside of the substrate, a plurality of power supply and grounding wiring layers (13, 14) and a plurality of through-hole wires (12) for conductively connecting each of said input

and output pins (11) provided on the under **surface** of the **substrate** to the upper **surface** of the **substrate**; multiple wiring layers (2) over the upper surface of said alumina ceramic substrate (1), having a plurality of thin-film conductive wiring layers (24, 25), an insulating layer or layers (21, 22, 23) made of organic high polymer, sandwiched between said thin-film conductive wiring layers to insulate these layers from each other, a plurality of via holes (27, 28, 29) in said insulating layer or layers for conductively connecting said wiring layers to one another, and a plurality of surface terminal pads (26) for connecting leadless **chip** carriers (3) formed over the top layer, and so structured that each of said through-hole wires (12) in the alumina ceramic substrate (1) and each of said surface terminal pads (26) can be mutually connected in any desired combination through said thin-film conductive wiring layers and via-holes; and said plurality of leadless **chip** carriers (3) being arranged over the upper surface of said multiple wiring layers (2), and being equipped inside with at least one tape automated bonding **IC chip** (32) face down, each **chip** carrier (3) having a **chip** carrier substrate (31) with a plurality of grid-shaped **chip** carrier terminals (34) provided on its under surface and a **chip** carrier cover (33) made of a highly heat-conductive material, with the dies of the **IC chips** (32) directly connected to it by means of a bonding adhesive (35), wherein each of said upper surface terminal pads (26) of the wiring layers (2) and each of the **chip** carrier terminals (34) are mutually connected. (20pp)

Abstract (Equivalent): US 4744007 A

The multichip package comprises a substrate having a grid of input and output pins disposed on an under surface, with the power supply and grounding wire layers embedded in the **substrate**. An upper **surface** of the **substrate** has a number of thin wire layers separated by at least one insulating layer, and a

number of via holes in the insulating layer permit **conductive interconnection** of the wire layers. A number of leadless **chip** carriers on the upper have tape automated bonding leads that are inner lead bonded to the substrate.

The **chips** are directly connected to the substrate and have a number of **chip** carrier terminals on an under surface that connect to the terminal pads. The **chip** carrier has a cover made of highly heat conductive material that contacts the back side of at least one mounted **chip**.

USE - Data processing and communications systems.

(11pp)

US 4652970 A

The multichip package is comprised of a substrate having a grid of input and output pins disposed on an under surface.

Power supply and grounding wire layers are embedded in the **substrate**. An upper **surface** of the **substrate** has a series of thin wire layers separated by an insulating layer.

Holes in the insulating layer permit **conductive interconnection** of the wire layers. Leadless **chip** carriers on the upper layer have tape automated bonding leads that are inner lead bonded to the substrate.

The **chips** are directly connected to the substrate and use **chip** carrier terminals on an under surface for connection to the terminal pads.

The **chip** carrier has a cover made of highly heat conductive material that contacts the back side of at least one mounted **chip**

USE/ADVANTAGE - For data processing and communications systems. Ensures high signal propagation speed.
(13pp

61/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014435957
WPI Acc No: 2002-256660/200230
XRAM Acc No: C02-076375
XRPX Acc No: N02-198650
Semiconductor chip package for electronic image sensor die comprises body with **surface** opening exposing cavity, **first** shelf formed along cavity perimeter, semiconductor die, and optical lens
Patent Assignee: ATMEL CORP (ATME-N); LAM K M (LAMK-I)
Inventor: LAM K M
Number of Countries: 096 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200191193	A2	20011129	WO 2001US12344	A	20010410	200230	B
AU 200153547	A	20011203	AU 200153547	A	20010410	200230	
US 20020006687	A1	20020117	US 2000577201	A	20000523	200230	
			US 2001943804	A	20010830		
US 6541284	B2	20030401	US 2000577201	A	20000523	200324	
			US 2001943804	A	20010830		
TW 501244	A	20020901	TW 2001111545	A	20010515	200334	

Priority Applications (No Type Date): US 2000577201 A 20000523; US 2001943804 A 20010830
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200191193	A2	E	28	H01L-031/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200153547	A	H01L-031/00	Based on patent WO 200191193
US 20020006687	A1	H01L-021/44	Div ex application US 2000577201
US 6541284	B2	H01L-027/148	Div ex application US 2000577201
TW 501244	A	H01L-023/28	

Abstract (Basic): WO 200191193 A2
Abstract (Basic):
NOVELTY - A semiconductor chip package comprises a body with a surface opening exposing a cavity; first shelf formed along the perimeter of the cavity; semiconductor die having light receiving area formed on a surface; and optical lens on a second shelf. The optical lens is held a predetermined focal distance from the die by an adhesive having controllably activated curing stage.
DETAILED DESCRIPTION - A semiconductor chip package (80) comprises:
(i) body having a surface opening exposing a cavity;
(ii) first shelf formed along the perimeter of the cavity and protruding inwardly from the cavity walls, the underside of the first shelf forming a partial ceiling for a chamber within the cavity and the edge of the first shelf forming an aperture to the chamber;
(iii) semiconductor die having a light receiving area formed on a surface and facing the aperture; and
(iv) optical lens (89) on a second shelf.

The optical lens is held a predetermined focal distance from the die by an adhesive having a controllably activated curing stage.

An INDEPENDENT CLAIM is also included for a method of constructing a chip package for an integrated circuit image sensor die comprising:

(a) fastening the image sensor die to a base section of the chip package, the chip package further having a first shelf forming an aperture over the image sensor die;

(b) applying an adhesive having controllably activated curing stage on the first shelf;

(c) placing an optical lens on the adhesive such that the optical lens is freely movable;

(d) electrically coupling the image sensor die to focus testing equipment;

(e) activating the image sensor die and adjusting the position of the lens to identify its focal distance to a predetermined target plane; and

(f) activating the curing stage of the adhesive to hold the optical lens in the focal distance.

USE - Semiconductor chip package is used for an electronic image sensor die.

ADVANTAGE - The image module assembly is of reduced complexity. Cost associated with the construction of an imaging assembly is reduced. The invention also provides higher reliability for the overall imaging module assembly of camera. It also allows fabrication of a miniature camera for portable electronics, e.g. cellular phone, pagers, or PC cameras.

DESCRIPTION OF DRAWING(S) - The figure is a perspective view of an image sensing integrated circuit (IC) chip package.

IC chip package (80)
Filter glass (87)
Optical lens (89)
pp; 28 DwgNo 6/17

61/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014432686
WPI Acc No: 2002-253389/200230
Related WPI Acc No: 2000-105339; 2002-178943; 2002-461554
XRAM Acc No: C02-075802
XRPX Acc No: N02-195498
Fabrication of semiconductor devices involves adhesively fixing glass plate to **substrate surface**, applying sealant material to substrate's second side, forming contact holes via the glass plate, and metallizing the glass plate
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: FARNWORTH W M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6284573	B1	20010904	US 9882745	A	19980521	200230	B
			US 99388033	A	19990901		

Priority Applications (No Type Date): US 9882745 A 19980521; US 99388033 A 19990901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6284573	B1		12	H01L-021/301	Cont of application US 9882745 Cont of patent US 6008070

Abstract (Basic): US 6284573 B1
Abstract (Basic):
NOVELTY - Semiconductor devices are fabricated by providing semiconductor devices having circuit(s) and **bond pads**, adhesively fixing a glass plate to a **substrate active surface**, separating the devices after processing, applying a sealant material to a second side of the substrate, forming contact holes through the glass plate, metallizing the glass plate and singulating the devices.

DETAILED DESCRIPTION - Fabrication of semiconductor devices involves providing a semiconductor wafer substrate having first and second sides, and semiconductor devices formed on the substrate with street areas (22). Each semiconductor device has circuit(s) and **bond pads** on the first side. The **bond pads** are connected to the circuits.

A first glass plate (30) is adhesively secured to the first side of the substrate. It has an exterior and parallel interior surface. An exterior **surface** of the **first** plate is flattened, planarized, and polished in correlation with the second side of the substrate after fixing the first glass plate to the first side of the substrate with adhesive. A thickness of the substrate is reduced by removing a portion of the second side.

The devices are separated by removing substrate material in the street areas. They remain fixed to the first plate. A sealant material is applied to the second side of the substrate.

An array of contact holes (50) is formed and extends through the first plate to the **bond pads**. A metal is deposited on the exterior **surface** of the **first** plate to form a pattern of

conductive leads for connecting the **bond pads** to the metallized exterior **surface** of the **first** plate.

The devices are singulated by separation in the street areas.

USE - For fabricating semiconductor devices, especially ultra-thin packaged devices for use in small electronic consumer products.

ADVANTAGE - The inventive method provides hermetically sealed package, and allows the use of an unground and inexpensive glass plate material. The use of the photo-etchable glass obviates a re-pattern step before overlying the first glass plate. It eliminates the need to scribe the substrate before metallization. It results in lower trace resistance and parasitic losses as well as shorter traces for increased speed. The metallization eliminates the need to add a solder mask-limiting layer after bump metallization.

DESCRIPTION OF DRAWING(S) - The figure is a partial cross-sectional view of a wafer of semiconductor chips.

Sealant adhesive (20, 38)
Street areas (22)
First glass plate (30)
Second glass plate (40)
Contact holes (50)
pp; 12 DwgNo 9/11

61/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013777575
WPI Acc No: 2001-261786/200127
XRPX Acc No: N01-187140
Electrooptical apparatus for e.g. liquid crystal panel, has electroconductive contacting element to electrically connect **bonding pads** formed on chip installation and pad attachment surface
Patent Assignee: SHENG M D (SHEN-I); SHEN M (SHEN-I)
Inventor: SHEN M
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001051290	A	20010223	JP 99321094	A	19991111	200127	B
TW 415049	A	20001211	TW 99113398	A	19990805	200128	
US 6307270	B1	20011023	US 99401099	A	19990922	200165	

Priority Applications (No Type Date): TW 99U213224 U 19990805; TW 99113398 A 19990805
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001051290	A		6	G02F-001/1345	
TW 415049	A			H01L-023/02	
US 6307270	B1			H01L-023/48	

Abstract (Basic): JP 2001051290 A
Abstract (Basic):
NOVELTY - **Bonding pads** (31) are formed on pad attachment surface (32) of a transparent glass substrate (3). **Bonding pads** (52) formed on installation surface (51) of a semiconductor chip (5), are electrically connected to the **bonding pads** (31) by the electroconductive contacting element (45).
DETAILED DESCRIPTION - Several through-holes are formed on the **bonding pads** (31). An insulating tape (4) has bonding surface (41) which is **bonded** with the **pad attachment surface** of the **glass substrate**. The electroconductive contacting element is attached in space formed between the walls of through-hole and **bonding pad** (31). The installation surface is bonded to the bonding surface (42) of the insulating tape. An INDEPENDENT CLAIM is also included for manufacturing method of electrooptical apparatus.
USE - For e.g. liquid crystal panel. Also for charge coupled device (CCD), light emitting diode (LED).
ADVANTAGE - Since the electrical connection of **bonding pads** is performed by electroconductive contacting element instead of conducting wire, a wire jointing machine is not needed. Hence manufacturing cost is reduced greatly.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of manufacturing process of electrooptical apparatus.
Transparent glass substrate (3)
Insulating tape (4)
Semiconductor chip (5)
Bonding pad (31)
Pad attachment surface (32)

Bonding surfaces (41,42)
Electroconductive contacting element (45)
Installation surface (51)
pp; 6 DwgNo 3/7

61/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013546630
WPI Acc No: 2001-030836/200104
XRAM Acc No: C01-009265
XRPX Acc No: N01-024088
Forming semiconductor device test carrier includes use modified circuit board that performs failure analysis of semiconductor device
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHIU C; HSIEH C; WU W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6127833	A	20001003	US 99225382	A	19990104	200104	B

Priority Applications (No Type Date): US 99225382 A 19990104
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6127833	A		9	G01R-031/02	

Abstract (Basic): US 6127833 A
Abstract (Basic):

NOVELTY - Semiconductor device test carrier is formed by providing an off-the-shelf printed circuit board which is modified to receive a semiconductor device and to provide test accessibility to both the top and bottom surfaces of the device.

DETAILED DESCRIPTION - A semiconductor device test carrier is made by using a modified printed circuit board (PCB) and machining a rectangular cavity that is positioned concentric and within a conductive ground trace formed on the top surface of the PCB. A ruling pattern of conductive wire **bond pads** is formed in a linear array on each of four sides encircling the power trace. An interstitial ball pad array encircling the conductive wire **bond pads** connects with the bottom surface by conductive vias communicating with another interstitial ball array at the bottom surface. A **glass** plate is **attached** with an adhesive to the underside of the insulated substrate to form a transparent bottom-supporting surface for the rectangular cavity. A semiconductor device is placed into the cavity of the substrate, and its backside is adhesively bonded to the glass plate, thus baring both backside and frontside for EMMI failure analysis. Conductive wire and wire **bonder** connect the **bonding pads** of the device to appropriate wire bond fingers and traces of the substrate. An encapsulant encapsulates all wire connections between the device and the device test carrier.

USE - For use in forming a semiconductor device test carrier.

ADVANTAGE - The improved method expedites prototype functional testing, thus reducing product time to market. The test package is fabricated at a cost that is lower than that of other packages. It utilizes a modified PCB that provides test accessibility to both the top and bottom surfaces of the device.

pp; 9 DwgNo 0/7

61/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012734831
WPI Acc No: 1999-540948/199945
XRAM Acc No: C99-158100
XRPX Acc No: N99-400895
Reduction of parasitic capacitance between a semiconductor metallization pattern and printed circuit metallization
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS AB (PHIG); US PHILIPS CORP (PHIG)
Inventor: DEKKER R; MAAS H G R; VAN DEURZEN M H W A
Number of Countries: 020 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9945588	A2	19990910	WO 99IB254	A	19990215	199945	B
EP 985228	A1	20000315	EP 99901843	A	19990215	200018	
			WO 99IB254	A	19990215		
US 6177707	B1	20010123	US 99258430	A	19990226	200107	
JP 2001526842	W	20011218	JP 99544437	A	19990215	200203	
			WO 99IB254	A	19990215		

Priority Applications (No Type Date): EP 98200644 A 19980302
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9945588	A2	E	11	H01L-021/76	
Designated States (National): JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 985228	A1	E		H01L-021/76	Based on patent WO 9945588
Designated States (Regional): DE FR GB IT NL					
US 6177707	B1			H01L-029/10	
JP 2001526842	W		16	H01L-027/12	Based on patent WO 9945588

Abstract (Basic): WO 9945588 A2
Abstract (Basic):

NOVELTY - A device comprises a glass supporting body on which an insulated substrate is attached. The insulating layer is provided, on its **first** side, with a **surface** on which a semiconductor element is formed, and on which a metallization with a pattern of conductor tracks is provided. An insulating layer having a dielectric constant below 3 is provided between the metallization and the adhesive layer.

DETAILED DESCRIPTION - The device comprises a glass supporting body onto which an insulated substrate is attached by means of a layer of adhesive. The insulating layer is provided, on its first side facing the supporting body, with a surface on which a semiconductor element is formed in a layer of semiconductor material, and on which a metallization with a pattern of conductor tracks is provided. An insulating layer having a dielectric constant epsilonr below 3 is provided between the metallization formed on the substrate and the layer of adhesive.

USE - A semiconductor device comprising semiconductor elements and associated metallization **attached** to a **glass** supporting substrate, particularly suitable for high frequency signal processing applications.

ADVANTAGE - The power consumption of the device is reduced by reducing parasitic capacitances between the metallization of the semiconductor device and the metallization on the printed circuit board by more than 40%.

DESCRIPTION OF DRAWING(S) - The diagram shows a sectional representation of an embodiment of the semiconductor device.

Insulating Substrate (3)
Adhesive Layer (2)
Glass Supporting Body (1)
Semiconductor Material (6)
Semiconductor Element (7)
Metallization (8)
Conductors (9)
pp; 11 DwgNo 1/7

61/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

00736722
LIQUID CRYSTAL DISPLAY DEVICE

PUB. NO.: 56-057022 [JP 56057022 A]
PUBLISHED: May 19, 1981 (19810519)
INVENTOR(s): OGUCHI KOICHI
YAZAWA SATORU
NAGATA MITSUO
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-133835 [JP 79133835]
FILED: October 17, 1979 (19791017)
JOURNAL: Section: P, Section No. 72, Vol. 05, No. 115, Pg. 111, July 24, 1981 (19810724)

ABSTRACT

PURPOSE: To obtain a high-reliability and small-size liquid crystal display device where the man-hour is small, by using the mixture of a metal ball of the same diameter as the panel gap and an adhesive as the sealing material of both substrates belwo, in the liquid crystal **panel** using the **glass** substrate and the semiconductor substrate.

CONSTITUTION: **Bonding pad** part **surface** 18 on semiconductor **substrate** 16 including the liquid crystal driving circuit is covered with an Au thin film or a bump. Driving electrode 21 and nesa wiring 20 are formed on upper glass substrate 19. The mixture of Au ball 22 of the same diameter as the liquid crystal panel gap and adhesive 23 is used as the sealing material of substrates 19 and 16. Thus, nesa wiring 20 and **bonding pad** part 18 are connected by the Au ball without adopting the conventional connection method where the man-hour dependent upon wire bonding is large.

67/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015496247
WPI Acc No: 2003-558394/200352
Related WPI Acc No: 2003-491712
XRAM Acc No: C03-150290
XRPX Acc No: N03-443975
Shielding of circuit from stray magnetic fields comprises providing **integrated circuit** structure and applying first magnetic field shielding material to a portion of a **first surface**
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: KATTI R R; SPIELBERGER R K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030098469	A1	20030529	US 2000668922	A	20000925	200352 B
			US 2002314377	A	20021206	

Priority Applications (No Type Date): US 2000668922 A 20000925; US 2002314377 A 20021206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030098469	A1		8	H01L-031/328	Div ex application US 2000668922 Div ex patent US 6515352

Abstract (Basic): US 20030098469 A1
Abstract (Basic):
NOVELTY - A circuit is shielded from stray magnetic fields by providing **integrated circuit** structure having magnetizable material with its magnetization orientation confined to magnetization plane, the structure having a **first surface** parallel to the plane, and applying first magnetic field shielding material to a portion of the **first surface**.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(1) a method of protecting an **integrated circuit** magnetoresistive memory comprising providing a die (12) for the memory and forming a magnetic shield on a surface(s) of the die such that the shield is parallel to the magnetization plane; and
(2) a method of assembling an **integrated circuit** comprising providing the die for the circuit and providing the shield adapted to fit within a die cavity of a package for the circuit and using a bonding material to bond the shield to the die where the bonding material is compatible with high assembly temperatures consistent with assembly of light-reliability hermetic packages.
USE - Used to shield circuit from stray magnetic fields.
ADVANTAGE - The method provides simple, lightweight, economical shielding arrangement for **integrated circuits**.
DESCRIPTION OF DRAWING(S) - The figure shows a top plan view of the shielding arrangement.
Circuit die (12)
Bonding pads (20)
Ceramic package (30)
pp; 8 DwgNo 1/5

67/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015403896
WPI Acc No: 2003-466036/200344
XRAM Acc No: C03-124228
XRPX Acc No: N03-370695
Plating of metallic material on surface of dielectric material involves dipping surface of the dielectric material in solution containing catalytic metal particles having a slight electrostatic dipole
Patent Assignee: CUSTOM ONE DESIGN INC (CUST-N)
Inventor: KULINETS J M; NUYTKENS P R; POPEKO I E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030011049	A1	20030116	US 2001904306	A	20010712	200344	B

Priority Applications (No Type Date): US 2001904306 A 20010712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030011049	A1		24	H01L-023/495	

Abstract (Basic): US 20030011049 A1
Abstract (Basic):

NOVELTY - A metallic material is plated on surface of dielectric material by dipping the surface of the dielectric material in a solution containing catalytic metal particles having a slight electrostatic dipole, and placing the dielectric material surface in metal salt solution in metastable equilibrium with a reducing agent.

DETAILED DESCRIPTION - Plating of a metallic material on surface of dielectric material comprises dipping the surface of the dielectric material in a solution containing catalytic metal particles, which have a slight electrostatic dipole when in solution to held those particles attach to the dielectric material's surface.

The surface of dielectric material is placed in metal salt solution in metastable equilibrium with a reducing agent so as to cause the metal to be plated upon the surface of the dielectric material containing the catalytic metal particles by a process of electroless plating.

INDEPENDENT CLAIMS are also included for:

(a) an electrical circuit comprising dielectric layers comprising latex, and layers of electrically conductive material patterned to form multiple electrical interconnects;

(b) a multichip module comprising **integrated circuits** mounted on a substrate, dielectric layers of flexible dielectric material, and layers of electrically conductive material patterned to form multiple electrical interconnects between **bonding pads** on different **integrated circuits**; and

(c) a method of manufacturing multichip module comprising placing a frame (100) having holes on **first** flat **surface**, placing **integrated circuit chips** through frame, **removing** the **first substrate** from the frames and **chips**, placing layers of dielectric on top of the frames and **chips**, using photolithographic techniques to etch vias through dielectric layer to allow contact to conductive **bonding pads** on individual **chips** or conductive paths on dielectric layer below, and using photolithographic technique to lay down

conductive material in vias and in desired conductive pathways on the currently to layer of dielectric material.

USE - For plating metallic material on dielectric material, used in interconnect circuitry and multichip modules.

ADVANTAGE - The method provides electrical connections that can withstand expansion and contraction due to heating and cooling of electronic components.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a plastic frame used to hold **chips** in position according to the method.

Frame (100)

Chips (114, 116)

Epoxy (118)

pp; 24 DwgNo 6/39

67/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015355533
WPI Acc No: 2003-416471/200339
XRAM Acc No: C03-110204
XRPX Acc No: N03-331956

Formation of optical subassembly in **integrated circuit** by diffusing chromium from electrically conducting lines proximate **bonding pads**, **bonding** optical device to **bonding pad**(s), and attaching substrate to carrier

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: COHEN M S; HERRON L W; INTERRANTE M J; LOMBARDI T E; RAY S K; SHINDE S L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020196996	A1	20021226	US 2001885791	A	20010620	200339	B

Priority Applications (No Type Date): US 2001885791 A 20010620
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020196996	A1		10	G02B-006/13	

Abstract (Basic): US 20020196996 A1
Abstract (Basic):

NOVELTY - An optical subassembly in an **integrated circuit** is formed by:

(1) diffusing chromium from electrically conducting lines proximate **bonding pads** to prevent solder wetting down lines;

(2) bonding an optical device to one of the **bonding pads**; and

(3) attaching a substrate to a carrier using a solder bond attachment

DETAILED DESCRIPTION - Formation of an optical subassembly in an **integrated circuit** includes:

(1) defining electrically conducting lines and **bonding pads** in a metallization layer on a substrate;

(2) depositing a passivation layer over the metallization layer;

(3) etching the passivation layer to remove the passivation layer from each **bonding pad** and a portion of the metallization layer associated with each **bonding pad**;

(4) diffusing chromium (Cr) from the lines proximate the **bonding pads** to prevent solder wetting down lines; bonding an optical device to one of the **bonding pads**; and

(5) attaching the substrate to a carrier utilizing a solder bond attachment.

AN INDEPENDENT CLAIM is also included for an optical subassembly comprising:

(1) a carrier having a first and second side;

(2) a ball grid array (BGA) depending from the second side;

(3) a cavity disposed in the first side; and

(4) a silicon optical bench (SiOB) having an optical device mounted thereon, the SiOB is electrically and mechanically connected to the **first** side utilizing **surface** mount technology (SMT) attachment, the cavity providing clearance for the optical device when connecting the SiOB to the carrier, the SiOB having a metallization layer providing both wire **bondable** and solder **bondable pads**.

USE - For forming an optical subassembly (claimed) in an **integrated circuit**.

ADVANTAGE - The invention reduces the costs of not only the material, but also the complexity of the fabrication and the cost of the assembly, while maximizing operating performance. It allows both wire bond attachment of optical devices, as well as solderable metallurgy on the SiOB for attaching to the **chip** carrier.

DESCRIPTION OF DRAWING(S) - The figure is a cross sectional view of a silicon optical bench module having a flip-**chip** bonded laser diode.

SiOB (20)

Passivation layer (50)

Bond pads (100, 108)

Solder bumps (104)

pp; 10 DwgNo 4/4

67/3,AB/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015292090

WPI Acc No: 2003-353023/200333

XRAM Acc No: C03-093022

XRPX Acc No: N03-281969

Semiconductor package has substrate of approximate planar plate with insulative layer with land holes in its inner circumference and conductive patterns, semiconductor die, conductive bumps, encapsulating portion, and terminals

Patent Assignee: AMKOR TECHNOLOGY KOREA INC (AMKO-N); LEE K W (LEEK-I); LEE S G (LEES-I); LEE S H (LEES-I); YANG Y (YANG-I)

Inventor: LEE S H; YANG J Y; LEE K W; LEE S G

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030006494	A1	20030109	US 2002186407	A	20020628	200333	B
KR 2003003539	A	20030110	KR 200139441	A	20010703	200333	

Priority Applications (No Type Date): KR 200173608 A 20011124; KR 200139441 A 20010703

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030006494 A1			35	H01L-023/02	
KR 2003003539 A				H01L-023/52	

Abstract (Basic): US 20030006494 A1

Abstract (Basic):

NOVELTY - Semiconductor package comprises a substrate of an approximate planar plate comprising:

(i) an insulative layer having land holes in its inner circumference and conductive patterns on its surface;

(ii) a semiconductor die;

(iii) conductive bumps for coupling the **bond pads** to **bond** fingers of the conductive patterns;

(iv) an encapsulating portion, and

(v) terminals fused to each land

DETAILED DESCRIPTION - Semiconductor package comprises a substrate (110, 110', 110'') of an approximate planar plate comprising:

(i) an insulative layer having land holes (108, 108', 108'') formed in its inner circumference, and electrically conductive patterns formed at a surface of the insulative layer and including bond fingers formed in a central portion of the insulative layer and several lands (104, 104', 104'') for covering the land holes connected to the bond fingers;

(ii) a semiconductor die at a central portion of the substrate having **bond pads** formed at **one surface**;

(iii) conductive bumps for coupling the **bond pads** to the **bond** fingers among the conductive patterns of the substrate;

(iv) an encapsulating portion formed by applying an encapsulant to the **bond pads** of the semiconductor die, the conductive bumps, and the bond fingers of the conductive patterns; and

(v) terminals fused to each land of the substrate.

An INDEPENDENT CLAIM is also included for a method for manufacturing semiconductor package, which comprises providing an insulative layer of an approximately planar plate comprising a die cavity formed at its center and land holes formed at the periphery of the die cavity; coupling a conductive thin layer to the insulative layer; forming a substrate having electrically conductive patterns by etching the conductive thin layer in predetermined shape to form lands for covering the land holes and bond fingers extending to the inside of the die cavity; coupling an adhesive tape of an approximately planar plate to **one surface** of the **substrate**; locating a semiconductor die having **bond pads** inside the die cavity of the substrate; coupling conductive bumps to the **bond pads**; coupling the conductive bumps to the bond fingers; forming an encapsulating portion by applying an encapsulant to an inside of the die cavity to protect the **bond pads** of the semiconductor die, the conductive bumps, and the bond fingers of the **substrate** from external environment; **removing** the adhesive tape from the substrate; and coupling conductive balls to each land of the substrate.

USE - The semiconductor package may be used as a resin sealing package, a tape carrier package (TCP), a glass sealing package, or a metal sealing package. It can be an in-line type semiconductor package, e.g. dual in-line package or a pin grid array package; or a surface mount type semiconductor package, e.g. quad flat package, a plastic leaded **chip** carrier, a ceramic leaded carrier, or a ball grid array package.

ADVANTAGE - Partially inserting the solder balls into and connecting them to the land holes formed at the insulative layer of the

substrate reduce the height of the solder ball to the minimum, thus reducing the thickness of the stack type semiconductor package. The die protective layer prevents the damage of the **integrated circuits** due to a transmission of a laser during the laser marking process of the semiconductor package, thus improving the quality of the marking process providing ease of handling.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a semiconductor package.

Semiconductor packages (100, 100', 100'', 200)
Lands (104, 104', 104'')
Land holes (108, 108', 108'')
Substrate (110, 110', 110'')
Solder balls (140, 140', 140'')
pp; 35 DwgNo 2/19

67/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015266938
WPI Acc No: 2003-327867/200331
XRAM Acc No: C03-085210
XRPX Acc No: N03-262147

Fabrication of multi-**chip** module package involves **exposing bonding pads** of **chip** by forming patterned dielectric layer, and electrically connecting the **bonding pads** to substrate by electroplating to form metal layer

Patent Assignee: UNIMICRON TECHNOLOGY CORP (UNIM-N)
Inventor: CHENG D C H; CHENG J; FAN C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6506633	B1	20030114	US 200278212	A	20020215	200331	B

Priority Applications (No Type Date): US 200278212 A 20020215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6506633	B1		18	H01L-021/44	

Abstract (Basic): US 6506633 B1
Abstract (Basic):

NOVELTY - Fabrication of a multi-**chip** module (MCM) package involves **exposing bonding pads** of a **chip** by forming a patterned dielectric layer, and electrically connecting the **bonding pads** to a substrate by electroplating to form a metal layer.

DETAILED DESCRIPTION - Fabrication of a multi-**chip** module (MCM) package involves providing a substrate having an insulating core (302) and a conductive layer covering a bottom surface of the insulating core; forming a first opening in the **substrate** to **penetrate** through the insulating core and the conductive layer; adhering an adhesive tape to cover a surface of the conductive layer, where the first opening exposes a portion of a top surface of the adhesive tape; adhering a first **chip** (236) onto the exposed top surface of the adhesive tape, where the first **chip** has an active surface (236a) on which **bonding pads** (238) are formed and a back surface (236b) which is adhered onto the adhesive tape such that

the first **chip** is located firmly on the adhesive tape; forming a patterned dielectric layer (314a) to fill into the first opening to cover a portion of the exposed top surface of the adhesive tape, the active **surface** of the **first chip**, the **bonding pads** of the **chip**, and the insulating core, where the patterned dielectric layer has formed on it second openings to **expose** the **bonding pads** of the first **chip** and third openings to penetrate through the patterned dielectric layer, the insulating core, and the conductive layer; electroplating a metal layer on sidewalls of the second openings and the third openings and to cover the patterned dielectric layer; removing the adhesive tape to expose the conductive layer, the back **surface** of the **first chip**, and a portion of the patterned dielectric layer after the electroplating process; forming a patterned solder mask layer (324) to cover surfaces of the patterned metal layer (320a) and the patterned conductive layer (304a), where fourth and fifth openings are formed on the patterned solder mask layer to expose respectively a portion of the patterned metal layer and a portion of the patterned conductive layer; and performing a die adhering process to electrically connect at least a second **chip** to the patterned metal layer via the fourth openings.

USE - The method is used for fabricating a multi-**chip** module (MCM) package.

ADVANTAGE - The method improves the yield of the device, ensures good connection between the **chip** and the substrate, and prevents air bubble produced during the underfilling and molding processes. It can carry out the fabrications of the **chip** and the substrate simultaneously so that the flow of the fabricating process is simplified. The connection between the **chip** and the substrate is more reliable. The requiring accuracy of the fabrication is gradually from high to less, thus greatly improving the yield of the device.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view of fabricating an MCM package.

Chip (236)
Active surface (236a)
Back surface (236b)
Bonding pads (238)
Insulating core (302)
Patterned conductive layer (304a)
Patterned dielectric layer (314a)
Patterned metal layer (320a)
Patterned solder mask layer (324)
pp; 18 DwgNo 31/31

67/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015148121
WPI Acc No: 2003-208648/200320
XRPX Acc No: N03-166267
Method for forming conductive bumps on a substrate - capable of increasing the quality and reliability of flip **chip** package
Patent Assignee: PHOENIX PRECISION TECHNOLOGY CORP (PHOE-N)
Inventor: SHIU S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 481909	A	20020401	TW 2001111526	A	20010515	200320	B

Priority Applications (No Type Date): TW 2001111526 A 20010515
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 481909	A			H01L-023/48	

Abstract (Basic): TW 481909 A
Abstract (Basic):

NOVELTY - The present invention relates to a method for forming conductive bumps on a substrate. At first, there is provided an insulating **substrate** having a **surface** formed thereon a conductive film. A photoresist pattern is formed on the conductive film. The photoresist pattern defines a plurality of bump windows. Next, a bump is formed on the bump window. The photoresist pattern and part of conductive film out of the bump windows are **removed**. The **substrate** and the insulating substrate are bonded, wherein the substrate has been provided with a plurality of solder **pads** to **bond** with bumps of the insulating substrate. By heating and bonding, it is able to transfer the bumps on the insulating substrate to the **substrate**, and **remove** the insulating **substrate** thereby completing the process of forming conductive bumps on a substrate. The insulating substrate can be repeatedly used to form the bumps thereby completing a process of forming more conductive bumps on the substrate.

DwgNo 0/0

67/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015104973
WPI Acc No: 2003-165490/200316
XRAM Acc No: C03-042845
XRPX Acc No: N03-130642

Fabrication of semiconductor device by implanting impurities into exposed surface of gate insulating layer formed over first substrate, cleaving, and **bonding exposed** surface of the gate insulating layer to second substrate

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: ISHIDA E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6482725	B1	20021119	US 99149421	P	19990818	200316	B
			US 2000640083	A	20000817		

Priority Applications (No Type Date): US 99149421 P 19990818; US 2000640083 A 20000817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6482725	B1		7	H01L-021/26	Provisional application US 99149421

Abstract (Basic): US 6482725 B1
Abstract (Basic):

NOVELTY - Semiconductor device is fabricated by forming a gate

insulator layer over a major **surface** of a **first substrate**, implanting impurities into the exposed surface of the gate insulating layer, cleaving the implanted first substrate along a cleavage plane, providing a second **substrate**, **bonding** the **exposed surface** of the gate insulating layer to the **first** major **surface** of the **second substrate**.

DETAILED DESCRIPTION - Fabrication of a semiconductor device comprising;

(a) a gate insulator layer (4) and an overlying electrically conductive gate layer involves providing a first, p+ or n+ type semiconductor substrate (1) having opposed **first** and **second** major **surfaces** (2, 3) spaced apart by side surfaces;

(b) forming a gate insulator layer on the **first** major **surface** of the **first substrate**;

(c) implanting impurities into the exposed surface of the gate insulating layer, where the impurities pass through the gate insulating layer and penetrate into the underlying first semiconductor substrate for a depth below the **first** major **surface**, and the structural integrity of the first substrate is weakened at the depth;

(d) cleaving the impurity-implanted first substrate along a cleavage plane parallel to the **first** major **surface** and located at the depth;

(e) providing a second semiconductor substrate (8) of the same conductivity type as the first substrate and having opposed **first** and **second** major **surfaces** (9, 10); and

(f) **bonding** the **exposed** surface of the gate insulating layer of the cleaved first substrate to the **first** major **surface** of the **second substrate**, where the first semiconductor substrate forms an electrically conductive gate electrode in contact with the gate insulator layer, and dopant depletion of the first semiconductor **substrate** with attendant **penetration** of the dopant into the gate insulator layer is reduced or prevented.

USE - The method is used for the fabrication of a semiconductor device, e.g. metal oxide semiconductor, complementary metal oxide semiconductor transistors, and **integrated circuits** containing such transistors on a common semiconductor substrate. It is particularly used in fabricating high-density integration semiconductor devices with design features below 0.18 mum.

ADVANTAGE - The method manufactures semiconductor devices with improved processing methodology resulting in increased reliability, quality, and device performance. It minimizes or eliminates dopant depletion of the gate polysilicon layers and the resultant dopant penetration of underlying gate oxide layers.

DESCRIPTION OF DRAWING(S) - The figure illustrates in simplified cross-sectional form, of steps for forming improved gate electrodes.

First substrate (1)

First and second major **surfaces** of the **first substrate** (2, 3)

Gate insulator layer (4)

Second substrate (8)

First and second **surfaces** of **second substrate** (9, 10)

pp; 7 DwgNo 1/1

67/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015095236
WPI Acc No: 2003-155754/200315
XRAM Acc No: C03-040312
XRPX Acc No: N03-122902
Method for making an electrical structure, e.g. a space transformer, by performing laser etching operations on a workpiece, without removing the workpiece from the laser processing system
Patent Assignee: JOHNSON M T (JOHN-I)
Inventor: JOHNSON M T
Number of Countries: 097 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020111029	A1	20020815	US 2001268382	P	20010212	200315 B
			US 2001277118	P	20010319	
			US 2001277349	P	20010319	
			US 200276178	A	20020212	
WO 200264301	A2	20020822	WO 2002US4425	A	20020212	200315

Priority Applications (No Type Date): US 200276178 A 20020212; US 2001268382 P 20010212; US 2001277118 P 20010319; US 2001277349 P 20010319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020111029	A1		13	H01L-021/302	Provisional application US 2001268382
					Provisional application US 2001277118
					Provisional application US 2001277349
WO 200264301	A2	E		B23K-026/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20020111029 A1
Abstract (Basic):

NOVELTY - An electrical structure is made by forming fiducial(s) by laser etching, removing portions of conductive material by laser etching to form isolated conductive traces, laser etching alignment hole(s) to receive alignment pin(s), laser etching folding line(s), and singulating the electrical structure. All this takes place in a laser processing system without **removing** the **substrate.**

DETAILED DESCRIPTION - Method for making an electrical structure involves:

(1) preparing a database;

(2) placing a substrate, with an electrically insulating material and a first blanket layer of conductive material on its **first surface**, in a **first** laser processing system;

(3) forming fiducial(s) by laser etching;

(4) removing portions of the conductive material by laser etching to form isolated conductive traces;

(5) laser etching at least one alignment hole for receiving alignment pin(s);

(6) laser etching at least one folding line; and

(7) singulating the electrical structure.

The forming, removing, laser etching, and singulating steps are all performed in the first processing system.

USE - For making an electrical structure i.e. a space transformer (claimed) to provide an electrical bridge between the smallest features in one technology (e.g. pins of a probe card) and the largest features in another technology (e.g. **bonding pads** of an **integrated circuit**).

ADVANTAGE - The invention provides improved dimensional accuracy and cost-effective manufacturing, provides high density that results from the ability to form very narrow spaces, and allows electrical structures to be formed with less material than would be consumed by conventional methods. The structure is very simply manufactured, inexpensively created, high density, single-manufacturing-step component that can be made easily, economically and selectively both in very small quantities and in much larger batches if required. Extremely dense landscapes of conductors can be created that allow for the creation of electrical structures smaller in overall size than counterparts fabricated by conventional methods.

pp; 13 DwgNo 0/9

67/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015027222
WPI Acc No: 2003-087739/200308
XRAM Acc No: C03-022066
Method for fabricating ball grid array package having heat sink
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: CHO S D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002057516	A	20020711	KR 2001589	A	20010105	200308	B

Priority Applications (No Type Date): KR 2001589 A 20010105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002057516	A		1	H01L-023/12	

Abstract (Basic): KR 2002057516 A
Abstract (Basic):

NOVELTY - A method for fabricating a ball grid array(BGA) package having a heat sink is provided to increase production efficiency, by performing a process for attaching the heat sink in a substrate strip state while a **chip** mounting process of a package fabricating process is carried out.

DETAILED DESCRIPTION - A substrate strip has an upper surface and a lower surface opposite to the upper surface. **Chip** mounting holes(37) are formed in the **substrate** strip, **penetrating** the upper surface and the lower surface and separated from each other by a predetermined interval. A semiconductor **chip**(10) is attached to a surface of the heat sinks(40). The heat sinks are attached to the lower **surface** of the **substrate** strip, corresponding to the **chip** mounting holes so that the semiconductor **chip** is exposed to the **chip** mounting holes. A bonding wire(50) electrically connects the semiconductor **chip** with the substrate strip. Molding resin molds the semiconductor **chip** and the **bonding** wire **exposed** to the **chip** mounting holes on

the upper **surface** of the **substrate** strip to form a resin encapsulating part(60). Solder balls(70) are formed on the upper **surface** of the **substrate** strip on the circumference of the resin encapsulating part. The substrate strip is separated into individual BGA package.
pp; 1 DwgNo 1/10

67/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014967935
WPI Acc No: 2003-028449/200302
XRAM Acc No: C03-006536
XRPX Acc No: N03-022316
Packaging structure of image sensor comprises substrate including metal sheets, glue for sealing sheets, image sensing **chip** on which several **bonding pads** are formed, wirings, and transparent layer
Patent Assignee: CHEN L H (CHEN-I); CHEN W C (CHEN-I); CHENG C S (CHEN-I); HO M N (HOMN-I); LIU J (LIUJ-I); TU H W (TUHW-I); WU J (WUJJ-I)
Inventor: CHEN L H; CHEN W C; CHENG C S; HO M N; LIU J; TU H W; WU J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020096758	A1	20020725	US 2001768845	A	20010123	200302	B

Priority Applications (No Type Date): US 2001768845 A 20010123
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020096758	A1		6	H01L-023/12	

Abstract (Basic): US 20020096758 A1
Abstract (Basic):
NOVELTY - Packaging structure of image sensor comprises:
(A) a substrate including metal sheets and glue for sealing the sheets;
(B) an image sensing **chip** on which several **bonding pads** are formed within its concavity;
(C) wirings electrically connecting the **bonding pads** of the image sensing **chip** to **first** contacts of first **surface** of the **substrate**; and
(D) a transparent layer on the projecting edge of the **first surface**.
DETAILED DESCRIPTION - Packaging structure of an image sensor comprises:
(A) a substrate (10) including metal sheets (16), glue (18) for sealing the metal sheets, a **first surface** (20) with a periphery, and a **second surface** (22) opposite to the **first surface**, where the metal sheets are exposed to the outside via the **first surface** and the **second surface** to form **first** contacts (26) and second contacts (28), respectively, and a projecting edge (30) is provided on the periphery of the **first surface** of the **substrate** to form a concavity (32) above the substrate;
(B) an image sensing **chip** (12) on which several **bonding pads** (34) are formed within its concavity;
(C) wirings (15) electrically connecting the **bonding**

pads of the image sensing **chip** to the first contacts of the **first surface** of the **substrate** to electrically connect the image sensing **chip** to the substrate so that electrical signals from the image sensing **chip** are capable of being transmitted to the second contacts of the **second surface** of the **substrate**; and

(D) a transparent layer (14) arranged on the projecting edge of the **first surface** of the **substrate** so that the image sensing **chip** is capable of receiving the optical signals.

An INDEPENDENT CLAIM is also included for a method for packing an image sensor, comprising preparing a substrate; mounting the substrate; connecting **bonding pads** of the image sensing **chip** to the first contacts of the **first surface** of the **substrate** by several wirings; and mounting a transparent layer on the projecting edge on the **first surface** of the **substrate** to cover the image sensing **chip**.

USE - The packaging structure is used for packaging an image sensor.

ADVANTAGE - Manufacturing costs can be lowered and the signal transmission of the image sensing **chip** can be improved by making the transmission distances shorter. Since the substrate formed by sealing the metal sheets with the glue can be easily **cut**, several **substrates** can be manufactured by molding at the same time. This lowers manufacturing costs. The metal sheets of the **substrate** have smooth **surfaces**, therefore better electric contacting effects between the substrate and the circuit board can be obtained. The plastic material for forming the substrate is cheaper than the ceramic material used in the prior art, thus lowering packaging costs.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view showing the packaging structure of the image sensor.

Substrate (10)
Image sensing **chip** (12)
Transparent layer (14)
Wirings (15)
Metal sheets (16)
Glue (18)
First surface (20)
Second surface (22)
First contacts (26)
Second contacts (28)
Projecting edge (30)
Concavity (32)
Bonding pads (34)
pp; 6 DwgNo 1/4

67/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014930020
WPI Acc No: 2002-750729/200281
XRAM Acc No: C02-212849
XRPX Acc No: N02-591202

Deposition of material on metallization substrate, involves etching **substrate** until oxide is **removed** and surface is activated, rinsing in non-aqueous liquid, initiating plating when liquid remains on substrate

Patent Assignee: UNIV NAT IRELAND CORK (UYNA-N)
Inventor: BARRETT J; BOARDMAN J; GEARY E; MATHEWSON A; MURPHY P A; ROHAN J F
Number of Countries: 100 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200283980	A1	20021024	WO 2002IE44	A	20020411	200281	B
IE 82880	B	20030514	IE 2002264	A	20020411	200339	

Priority Applications (No Type Date): IE 2001365 A 20010412
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200283980	A1	E	17	C23C-018/18	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

IE 82880	B		C23C-018/16		

Abstract (Basic): WO 200283980 A1
Abstract (Basic):

NOVELTY - The semiconductor metallization substrate (1) is cleaned by etching, until oxide is removed and the **surface** is **activated**. The **substrate** is rinsed in a non-aqueous liquid to prevent re-oxidation. Electroless plating is initiated while some non-aqueous liquid remains on the substrate and the material is deposited. The operating temperature of the plating bath is higher than the boiling point of the liquid.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a semiconductor metallization substrate.

USE - For depositing material such as switch contact material on semiconductor substrate such as **integrated circuit** metallization substrate for complementary metal oxide semiconductor (CMOS) micromechanical switches.

ADVANTAGE - The electroless plating occurs only on the substrate and not on the other materials such as dielectric materials. Hence the deposition method has excellent selectivity. The oxides are **removed** and the **substrate** is **activated** by etching, thereby avoiding the need for a series of basic and acidic baths and need for exposing to metal salts. The substrate is not exposed to small mobile ions or additional metal ion such as fluoride ions, and the material is deposited by simple method.

DESCRIPTION OF DRAWING(S) - The figure shows a diagrammatic cross-sectional representation of silicon wafer with aluminum **bond pads** before and after nickel plating.

Semiconductor metallization substrate (1)
pp; 17 DwgNo 1/3

67/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014640375
WPI Acc No: 2002-461079/200249

Method for fabricating semiconductor **chip** package formed with solder ball
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM H G; KIM S Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002004356	A	20020116	KR 200038177	A	20000705	200249	B

Priority Applications (No Type Date): KR 200038177 A 20000705
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002004356	A		1	H01L-023/28	

Abstract (Basic): KR 2002004356 A
Abstract (Basic):

NOVELTY - A method for fabricating a semiconductor **chip** package formed with a solder ball is provided to enhance an adhesive strength between a solder ball and a substrate by preventing permeation of a sealing resin to a solder ball formation region.

DETAILED DESCRIPTION - A window(58) is formed on a substrate(52) in order to **penetrate** the **substrate**(52). An **active** face of a semiconductor **chip**(60) including a **bonding pad** (62) is adhered to an adhesive tape. The **bonding pad**(62) is **exposed** by the window(58). A metal line is used for connecting electrically a terminal(57) with the **bonding pad**(62) through the window(58). A shield tape is adhered to an upper face of the substrate(52). A solder ball formation **region** of the **substrate**(52) except for the window(58) and the terminal(57) is covered by the shield tape. A sealing portion(68) is formed by supplying a sealing resin through the shield tape. The shield tape is removed after the sealing portion(68) is formed. A semiconductor **chip** package(80) is completed by adhering a solder ball(70) to the solder ball formation region.

pp; 1 DwgNo 1/10

67/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014452383
WPI Acc No: 2002-273086/200232
XRPX Acc No: N02-212855
Failure analysis method of semiconductor device, involves **bonding pad** on semiconductor **chip** and output pad for analysis, by wire
Patent Assignee: NEC CORP (NIDE)
Inventor: OZAWA T
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001289905	A	20011019	JP 2000104457	A	20000406	200232	B
US 20020013009	A1	20020131	US 2001822368	A	20010402	200232	
US 6472234	B2	20021029	US 2001822368	A	20010402	200274	
JP 3424649	B2	20030707	JP 2000104457	A	20000406	200345	

Priority Applications (No Type Date): JP 2000104457 A 20000406

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001289905	A		5	G01R-031/26	
US 20020013009	A1			H01L-021/66	
US 6472234	B2			G01R-031/26	
JP 3424649	B2		5	G01R-031/26	Previous Publ. patent JP 2001289905

Abstract (Basic): JP 2001289905 A

Abstract (Basic):

NOVELTY - The heat spreader and micro solder balls are provided to top and bottom **surfaces** of silicon **substrate**. While performing failure analysis, the solder ball for BGA provided in undersurface of ceramic substrate, and ceramic **substrate** are **removed**, and then micro solder ball is removed to expose pad of silicon substrate, connected with output **pad** by **bonding** wires.

USE - For failure analysis of semiconductor device of flip-**chip** type.

ADVANTAGE - Since failure analysis is performed by **bonding** required **pads**, effective electric and physical failure analysis of semiconductor device is enabled.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart of failure analysis process. (Drawing includes non-English language text).

pp; 5 DwgNo 1/9

67/3,AB/14 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014445975

WPI Acc No: 2002-266678/200231

Related WPI Acc No: 2002-153679

XRAM Acc No: C02-079389

XRPX Acc No: N02-207217

Removal of patterned photoresist layers from semiconductor substrates involves stripping photoresist layer by wet chemical treatment and preheating substrate at elevated temperatures before dry ash step

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)

Inventor: LIN C; PENG C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010019894	A1	20010906	US 99252627	A	19990218	200231	B
			US 2001838748	A	20010420		

Priority Applications (No Type Date): US 99252627 A 19990218; US 2001838748 A 20010420

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010019894	A1		13	H01L-021/302	Div ex application US 99252627 Div ex patent US 6251794

Abstract (Basic): US 20010019894 A1

Abstract (Basic):

NOVELTY - A photoresist layer (7, 8) coated on an underlying layer is **removed** from a semiconductor **substrate** by stripping the photoresist layer from the substrate by a wet chemical treatment. The

substrate is preheated to release a photoresist residue imbedded within the underlying layer. The substrate is then dry ashed with an oxygen plasma to remove the photoresist residue from the substrate (1).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a method of preparation for alloying an array of **bond pads** (2) on a semiconductor **substrate** overlaid with a **passivation** layer (3) underlying a patterned photoresist layer comprising (i) etching the passivation layer to form an array of contact openings to the array of **bond pads**, and (ii) removing the photoresist layer using the above procedures; and

(B) a preheating dry ash integrated multiple modular chamber vacuum processing system for removing the photoresist from the semiconductor substrate comprising (i) interconnected vacuum chambers, (ii) substrate receiving-device within one of the vacuum chambers, (iii) substrate transferring-device within one of the vacuum chambers, (iv) substrate preheater within one of the vacuum chambers, (v) oxygen plasma dry ashing device within one of the vacuum chambers, and (vi) substrate cooling device within one of the vacuum chambers.

USE - The method is used for removing photoresist layers from semiconductor substrates, useful in the fabrication of **integrated circuit** devices.

ADVANTAGE - The method eliminates the post alloy oxygen plasma dry ash step found in the conventional method and results in cost savings, a shorter manufacturing cycle time and the elimination of potential plasma damage or degradation to the devices on the substrate due to extra oxygen plasma dry ash operations.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor substrate.

Substrate (1)
Bond pad (2)
Passivation layer (3)
Photoresist layer (7, 8)
pp; 13 DwgNo 1/14

67/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014394859
WPI Acc No: 2002-215562/200227
Related WPI Acc No: 2002-224236
XRAM Acc No: C02-065809
XRPX Acc No: N02-165117

Mounting of one or more wire bond **integrated circuit chips** by creating interface substrate overlying metal substrate comprises creating build up multilayer layer over interconnect layer

Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010046725	A1	20011129	US 99389634	A	19990903	200227 B
			US 2001900558	A	20010709	
US 6455926	B2	20020924	US 99389634	A	19990903	200266
			US 2001900558	A	20010709	

Priority Applications (No Type Date): US 99389634 A 19990903; US 2001900558 A 20010709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010046725	A1		12	H01L-021/44	Div ex application US 99389634
US 6455926	B2			H01L-023/02	Div ex application US 99389634 Div ex patent US 6277672

Abstract (Basic): US 20010046725 A1
Abstract (Basic):

NOVELTY - Mounting of one or more wire bond **integrated circuit chips** by creating an interface substrate overlying a metal substrate comprises: providing wire bond **chip**(s) and metal substrate; creating build up multilayer; masking and etching the substrate; selectively creating openings; inserting **chips** into openings; wire bonding the **chips**; and inserting solder balls to ball grid array solder connections.

DETAILED DESCRIPTION - Mounting of one or more wire bond **integrated circuit chips** (16) by creating an interface substrate overlying a metal substrate (14) comprises:

(a) providing one or more wire **bond chips** having **pads** for wire **bond** connections;

(b) providing a metal substrate having **first** and **second surfaces** (24, 26);

(c) cleaning the **first surface** of the metal **substrate**;

(d) depositing a layer of dielectric over the **first surface**;

(e) depositing an interconnect layer over the dielectric layer to form the first layer of an interconnect substrate (12);

(f) creating a build up multilayer (BUM) layer over the interconnect layer to form the second layer of interconnect substrate;

(g) masking and etching the **second surface** of the metal **substrate** to create one or more openings (28) for the insertion of one or more **bond chips** to furthermore **expose** portions of the dielectric within the openings;

(h) selectively creating openings in the exposed dielectric to provide electrical access and heat **removal** to the interconnect **substrate** for the wire bond **chip**(s);

(i) subdividing the metal substrate into individual wire bond substrates;

(j) coating the exposed dielectric of the individual wire bond substrates with a layer of adhesive (17);

(k) inserting wire bond **chip**(s) into opening(s) for the insertion of the wire bond **chips** in the individual wire bond substrates where the wire bond **chips** overlay the adhesive coating;

(l) wire bonding the wire bond **chips** to the selectively created openings in the dielectric;

(m) inserting a molding compound over the wire bond **chip**(s) within the opening(s) for the insertion of the wire bond **chips**;

(n) coating the BUM layer as a solder mask;

(o) exposing the metal pads within the BUM layer to create openings for the ball grid array (BGA) solder connections; and

(p) inserting and attaching solder balls (10, 11) to the BGA solder connections.

An INDEPENDENT CLAIM is also included for a structure for mounting one or more wire bond **IC chips** by creating an interface

substrate overlying a metal substrate comprising:
(i) metal substrate having **first** and **second surfaces**;
(ii) layer of dielectric with a thickness of 10-50 microns deposited over the **first surface**;
(iii) thin film interconnect layer deposited over the layer of dielectric to form a first layer of an interconnect substrate;
(iv) BUM layer created over the interconnect layer to form the second layer of an interconnect substrate; (v) opening(s) for the insertion of wire bond **chip**(s) created by masking and etching the **second surface** of the metal **substrate** to furthermore create exposed portions of the dielectric within the openings;
(vi) openings selectively created in the exposed dielectric to provide electrical access and heat transfer to the interconnect substrate for the wire bond **chip**(s);
(vii) individual wire bond substrates created by subdividing the metal substrate;
(viii) layer of adhesive containing thermally conductive epoxy such as thermoset or thermoplastic epoxy created by coating the exposed dielectric of the individual wire bond substrates;
(ix) wire bond **chip**(s) inserted into the opening(s) for the insertion of the wire bond **chips** in the individual wire bond substrates where the wire bond **chips** overlay the adhesive coating;
(x) wire bonds for the wire bond **chips** to the selectively created openings in the dielectric;
(xi) molding compound inserted over the wire bond **chip**(s) and within the opening(s) for the insertion of the wire bond **chips**;
(xii) coating over the BUM layer as a solder mask; (xiii) metal pads within the BUM layer created by etching to create openings for the BGA solder connections; and
(xiv) solder balls inserted and attached to the BGA solder connections.
USE - The method is used for mounting one or more wire bond **integrated circuit chips** to create packaging substrates that are used for wire bonded semiconductor devices.
ADVANTAGE - The method is inexpensive and reliable for high-density wire bond semiconductor device manufacturing. The wire bond package significantly improves the cooling of the **IC** device that is mounted. The method provides for high pin fan-out for wire bond semiconductor devices. The need for counter-balancing the effects of thick layers of dielectric used in conventional high-density wire bond semiconductor device manufacturing is eliminated. The method provides an initial surface with good planarity for the creation of high-density wire bond semiconductor structures. The structure used for mounting the wire bond **IC chip**(s) is devoid of warpage and dimensional variations during high temperature or wet chemical processing for the creation of high-density wire bond semiconductor structures.
DESCRIPTION OF DRAWING(S) - The figure shows a single **chip** wire bond **chip** package with two interconnect layers.
Solder balls (10, 11)
Interconnect substrate (12)
Metal substrate (14)
Wire bond **chip** (16)
Adhesive layer (17)
First and **second surfaces** (24, 26)
Opening(s) (28)
pp; 12 DwgNo 1/3

67/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014122904
WPI Acc No: 2001-607116/200169
XRAM Acc No: C01-180355
XRPX Acc No: N01-453210
Device for photoelectric transport of charged materials in liquid environment for micro- and opto- electronic devices, has a substrate generating light induced current, conductor, permeation layer and light source to illuminate substrate
Patent Assignee: NANOGEN INC (NANO-N)
Inventor: EDMAN C F; FORMOSA R; GURTNER C; HELLER M J
Number of Countries: 025 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200153799	A1	20010726	WO 2001US926	A	20010112	200169	B
AU 200132779	A	20010731	AU 200132779	A	20010112	200171	

Priority Applications (No Type Date): US 2000489855 A 20000124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200153799	A1	E	119	G01N-015/00	
AU 200132779	A			G01N-015/00	Based on patent WO 200153799

Designated States (National): AU BR CA CN JP NZ
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200153799 A1
Abstract (Basic):

NOVELTY - A device (I) for effecting photoelectric transport of charged materials in liquid environment, has a substrate (S) capable of generating light induced current, a conductor contacting at least a part of **surface** of **substrate**, a permeation layer supported on other **surface** of **substrate** coupled to attachment entities, and a light source disposed to illuminate at least a part of S to induce the current.

USE - The device is useful for effecting photoelectric transport of charged materials in a liquid environment (claimed). The device is used for integration and manufacture of photonic and electronic array components. High bit density (large byte) 3 and 4-dimensional optical data storage material and devices and low density optical memory for applications in authentication, anti-counterfeiting and encryption of information in documents or goods, are developed. The devices are applied in fabricating light emitter arrays over large surfaces, in assembly of 2 or 3 dimensional photonic crystal structures and in manufacture of hybrid-integrated components including flat panel displays, medical diagnostic equipment and data storage systems.

ADVANTAGE - The system does not rely on pre-patterned microelectronic arrays. The techniques of the invention have wide use in manufacture of micro electronic and opto electronic devices. The self-assembly fabrication technique based on DNA polymers enables the micron, sub-micron or nanoscale devices to be fabricated densely on their mother substrates and then be redistributed in a pre-programmed fashion on to the host **substrate**, by **removing** the

requirement for conservation of relative device spacing during the device grafting process. The technique also enables to manipulate and orientate with respect to each other, a large number of nanoscale devices, allowing the selective positioning of bonding structures, such as gold, tin, or solder structures as **bondings pads**, e.g., to achieve low cost or unassisted die-to-die processing, e.g., for flip-**chip** applications.
pp; 119 DwgNo 0/52

67/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014065393
WPI Acc No: 2001-549606/200161
Related WPI Acc No: 2001-475231
XRAM Acc No: C01-163511
XRPX Acc No: N01-408267
Semiconductor **integrated circuit** device comprises wiring layers formed on semiconductor substrate through interlayer insulating film, **bonding pad**, first interlayer insulating film, and first plug
Patent Assignee: AOYAGI T (AOYA-I); HARA Y (HARA-I); KOBAYASHI H (KOBA-I); OGISHIMA A (OGIS-I)
Inventor: AOYAGI T; HARA Y; KOBAYASHI H; OGISHIMA A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010019180	A1	20010906	US 2000748163	A	20001227	200161 B
			US 2001811535	A	20010320	

Priority Applications (No Type Date): JP 99370790 A 19991227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010019180	A1		26	H01L-023/48	Div ex application US 2000748163

Abstract (Basic): US 20010019180 A1
Abstract (Basic):
NOVELTY - A semiconductor **integrated circuit** device comprises wiring layers formed on a semiconductor substrate through an interlayer insulating film, a **bonding pad** formed at an upper wiring layer, a first interlayer insulating film below the **bonding pad**, and a first plug formed in the first interlayer insulating film having a hole through which a first conductive film is buried.
DETAILED DESCRIPTION - A semiconductor **integrated circuit** device comprises wiring layers (26, 27) formed on a semiconductor substrate through an interlayer insulating film, a **bonding pad** formed at an upper wiring layer, a first interlayer insulating film (29) below the **bonding pad**, and a first plug (28) formed in the first interlayer insulating film. A first conductive film is buried in a hole (24) formed in insulating film, in which any wire connected to the first plug is not formed in a wiring below the first plug.
An INDEPENDENT CLAIM is also included for a method for manufacturing the above semiconductor **integrated circuit** device comprising:

(a) forming a wire in an element-forming **region** on semiconductor **substrate** and forming an interlayer insulating film on the wire;

(b) etching the first insulating film to form a first through-hole and etching the first region to form a hole;

(c) forming a barrier metal film on the first interlayer insulating including the inner surfaces of the hole and the inner surfaces of the through-hole and forming a first conductive film on the upper portion of the barrier metal film so that the first conductive film is buried in the hole and the first through-hole;

(d) **removing** the **first** conductive film from the upper portion of the first interlayer insulating film to form a first plug in the hole and also a second plug in the first through-hole; and

(e) etching a second conductive film formed on the upper portion of the first interlayer insulating film so that an uppermost wire is formed on the first interlayer insulating film and forming a **bonding pad** on the first interlayer insulating film in the **bonding pad**-forming region.

USE - Used as semiconductor **integrated circuit** device.

ADVANTAGE - The method provides formation of the plug in the interlayer insulating film, and the adhesion between the **bonding pad**. Thus, the interlayer insulating film is improved and the separation of the **bonding pad** is effectively prevented. The avoidance of forming any wire in the wiring layer below the **bonding pad**, prevents cracking of the insulating film due to impact during wire bonding.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view of a portion of semiconductor substrate forming the **integrated circuit** device.

Hole (24)
Wiring layers (26, 27, 30, 31)
Plug (28, 34)
Insulating film (29)
pp; 26 DwgNo 2/19

67/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014056573
WPI Acc No: 2001-540786/200160
Related WPI Acc No: 2002-413610
XRAM Acc No: C01-161315
XRPX Acc No: N01-401899

Semiconductor **chip** used as packaging **chip** includes **bonding pad** positioned on dielectric layer that is harder than a surrounding dielectric layer

Patent Assignee: HUANG Y (HUAN-I); LIU H (LIUH-I); UNITED MICROELECTRONICS CORP (UNMI-N)
Inventor: HUANG Y; LIU H
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010009297	A1	20010726	US 99293963	A	19990419	200160	B
			US 2001800574	A	20010308		
US 6388326	B2	20020514	US 99293963	A	19990419	200239	
			US 2001800574	A	20010308		

Priority Applications (No Type Date): US 99293963 A 19990419; US 2001800574 A 20010308
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010009297	A1		6	H01L-021/44	Div ex application US 99293963
US 6388326	B2			H01L-023/28	Div ex application US 99293963

Abstract (Basic): US 20010009297 A1
Abstract (Basic):

NOVELTY - A semiconductor **chip** includes a first dielectric layer (22), a second dielectric layer (24) positioned outside the area occupied by the first dielectric layer, and a **bonding pad** (26) on the first dielectric layer. The **bonding pad** is for electrically connecting an **integrated circuit** in the semiconductor **chip** with an external circuit. The first dielectric layer is harder than the second.

USE - As packaging **chip**.

ADVANTAGE - Peeling or rupture of the **bonding pads** during interconnection in the packaging process is avoided without affecting signal transmission speeds.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a **bonding pad** on a semiconductor wafer.

First dielectric layer (22)
Second dielectric layer (24)
Bonding pad (26)
pp; 6 DwgNo 7/9

67/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013991016
WPI Acc No: 2001-475231/200151
Related WPI Acc No: 2001-549606
XRAM Acc No: C01-142417
XRPX Acc No: N01-351769
Semiconductor **integrated circuit** device with improved **bonding** between **bonding pad** and interlayer insulating film below pad
Patent Assignee: HITACHI LTD (HITA); HITACHI MICON SYSTEM KK (HITA-N); HITACHI ULSI SYSTEMS CO LTD (HISC); AOYAGI T (AOYA-I); HARA Y (HARA-I); KOBAYASHI H (KOBA-I); OGISHIMA A (OGIS-I)
Inventor: AOYAGI T; HARA Y; KOBAYASHI H; OGISHIMA A
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010005624	A1	20010628	US 2000748163	A	20001227	200151	B
JP 2001185552	A	20010706	JP 99370790	A	19991227	200154	
KR 2001062344	A	20010707	KR 200075456	A	20001212	200175	
TW 503492	A	20020921	TW 2000126482	A	20001212	200337	
US 6573170	B2	20030603	US 2000748163	A	20001227	200339	

Priority Applications (No Type Date): JP 99370790 A 19991227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010005624	A1		26	H01L-023/48	
JP 2001185552	A		28	H01L-021/3205	

KR 2001062344 A H01L-021/60
TW 503492 A H01L-021/60
US 6573170 B2 H01L-021/00

Abstract (Basic): US 20010005624 A1
Abstract (Basic):

NOVELTY - Semiconductor **IC** device has wiring layers (13) on a substrate (1) through an interlayer insulating film and a **bonding pad** at an upper wiring layer. A first interlayer insulating film is provided beneath the **bonding pad**.

DETAILED DESCRIPTION - A first plug is formed in the first interlayer insulating film so that a first conductive film is buried in a hole formed in the interlayer insulation, where any wire connected to the first plug is not formed in a wiring layer beneath the first plug. AN INDEPENDENT CLAIM is also included for: a method of manufacturing the semiconductor **IC**, which comprises:

(a) forming a wire in an element forming **region** on a **substrate** (1);

(b) etching the first interlayer insulating film to form a through hole;

(c) forming a barrier metal film;

(d) **removing** the **first** conductive film from the upper portion of the first interlayer insulating film; and

(e) etching a second conductive film formed on the upper portion of the first interlayer insulation film.

USE - For improving **bonding** property between **bonding pad** and insulating film during semiconductor **IC** manufacture.

ADVANTAGE - Separation of the **bonding pad** is minimized.

DESCRIPTION OF DRAWING(S) - The drawing shows a sectional view of the semiconductor substrate.

substrate (1)
wiring layers (13)
pp; 26 DwgNo 2/19

67/3,AB/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013927098
WPI Acc No: 2001-411311/200144
XRPX Acc No: N01-304296
Method and device for transfer of elements such as **bonding pads** and **chips** from one substrate to another with step modification
Patent Assignee: COMMISSARIAT ENERGIE ATOMIQUE (COMS)
Inventor: BRUEL M
Number of Countries: 021 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2794443	A1	20001208	FR 996951	A	19990602	200144	B
WO 200075968	A1	20001214	WO 2000FR1507	A	20000531	200144	
EP 1183714	A1	20020306	EP 2000938871	A	20000531	200224	
			WO 2000FR1507	A	20000531		
JP 2003501827	W	20030114	WO 2000FR1507	A	20000531	200306	
			JP 2001502148	A	20000531		

Priority Applications (No Type Date): FR 996951 A 19990602
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2794443	A1		31	B65G-047/08	
WO 200075968	A1	F		H01L-021/00	
Designated States (National): JP US					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1183714	A1	F		H01L-021/00	Based on patent WO 200075968
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 2003501827	W		36	H01L-021/68	Based on patent WO 200075968

Abstract (Basic): FR 2794443 A1
Abstract (Basic):

NOVELTY - The set (20) for the transfer of elements arranged in a row with a step or spatial period d1, or in an array having rows and columns with steps (d1,d2) in directions (X,Y), respectively, comprises at least **one** receiving **surface** (7), and means for expansion and contraction, elastic or expandable, in particular in the form of a membrane (4), and traction (5) means, for changing the step in the first direction.

DETAILED DESCRIPTION - The set (20) is used for the transfer of elements as **bonding pads** and **chips** (10) from one substrate to the receiving substrate (3), and the contraction of membrane (4) on support (6) is realized by relaxing stressed membrane. The receiving surface can comprise a set of supports each with a receiving upper surface, and elastic means for expansion and contraction connected at least in the first direction, and also means for the application of traction at least in the first direction. The traction means comprise rods rigidly connected to the first and last supports in each row and column, and the supports are translationally mobile in parallel to columns and rows, respectively. The rods of traction system are rigidly connected to rings sliding on bars parallel to the direction of rods. The receiving surface on supports can be adapted to receive a liquid. The manufacturing method for N **chips** each having n **bonding pads** of given functions, each **chip** having n1 columns and n2 rows (n1.n2=n), from n monofunction **chips** each having N identical **bonding pads** arranged in n3 columns and n4 rows (n3.n4=n), from n monofunction **chips** each having N **bonding pads** P1 of function F1, and the last **chip** having N **bonding pads** Pn of function Fn, includes the following operations: (a) the transfer of **bonding pads** by a set comprising at least N receiving surfaces arranged in an array with n3 columns and n4 rows; (b) the action of expansion or contraction in the direction of rows to obtain a spacing of columns by a distance at least equal to n1 times the step d1; (c) the action of expansion or contraction in the direction of columns to obtain a spacing of rows at least equal to n2 times the step d2; (d) the transfer of **bonding pads** to the receiving substrate; (e) the repetition of operations (a) to (d) (n1-1) times, displacing each time the receiving substrate in the direction of rows by the step distance d1, to obtain the first rows of multifunction **chips** from monofunction **chips**; (f) the repetition of operations (a) to (e) (n2-1) times, displacing each time the receiving substrate in the direction of columns by the step distance d2, to obtain other rows of multifunction **chips**; and (g) the **cutting** of the receiving **substrate** according to design.

USE - In methods of transfer of elements, in particular **bonding pads** and **chips**, from one substrate to another, in manufacture of **integrated circuits**.

ADVANTAGE - The method can be used to make e.g. 900 bio **chips**, each of size 3x3 mm and having 225 **bonding pads** in 15 rows and 15 columns, from 225 monofunction arrays each comprising 900 identical **bonding pads** of size 200 x 200 micrometer in 30 rows and 30 columns.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of the device.

Substrate (3)
Membrane (4)
Traction means (5)
Support (6)
Receiving surface (7)
Chip (10)
Set (20)
pp; 31 DwgNo 5/11

67/3,AB/21 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013905067
WPI Acc No: 2001-389280/200141
Related WPI Acc No: 2002-009228
XRAM Acc No: C01-118664
XRPX Acc No: N01-286311
Direct contact through hole type wafer used for forming a wafer-level package has devices and contacts coupled to each other on both sides of the wafer
Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N); HAN C (HANC-I); HSUAN M C (HSUA-I)
Inventor: HAN T; SHIUAN M; HAN C; HSUAN M C
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010005046	A1	20010628	US 99260218	A	19990301	200141 B
			US 2001753735	A	20010102	
US 6323546	B2	20011127	US 99260218	A	19990301	200175
			US 2001753735	A	20010102	
TW 442873	A	20010623	TW 99100499	A	19990114	200206

Priority Applications (No Type Date): TW 99100499 A 19990114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010005046	A1		15	H01L-023/48	Cont of application US 99260218
US 6323546	B2			H01L-023/02	Cont of application US 99260218
					Cont of patent US 6252300
TW 442873	A			H01L-021/60	

Abstract (Basic): US 20010005046 A1
Abstract (Basic):

NOVELTY - Direct contact through hole type wafer has devices and contacts on both sides of the wafer. The contacts are coupled with the devices and bumps are formed on the contacts.

DETAILED DESCRIPTION - Direct contact through hole type wafer

structure comprises:

(a) a silicon-on-insulator substrate comprising first and second silicon substrates with a first insulation layer between them. At least one opening is formed in the second silicon **substrate** which **penetrates** through the first insulation layer into the first silicon substrate;

(b) at least one device on the first silicon substrate;

(c) a number of contact plugs positioned in the first silicon substrate and exposed by the opening;

(d) a number of dielectric layers and a number of patterned conductive layers which couple with the device and the contact plugs and a number of plugs in the dielectric layers. The dielectric layers and patterned conductive layers are alternately stacked on the first silicon substrate. At least one **bonding pad** is formed on the uppermost conductive layer and exposed by an uppermost conductive layer formed on the uppermost conductive layer;

(e) a second insulation layer positioned in the opening. The second insulation layer lies on the surface of the opening and exposes the contact plugs;

(f) a barrier layer which is positioned on the second insulation layer and is coupled with the contact plugs; and

(g) a metal layer which is positioned on the barrier layer.

INDEPENDENT CLAIMS are also included for the following:

(i) a direct contact through hole type wafer structure comprising: a substrate having **first** and **second surfaces**; at least **one** device positioned on the **first surface**; a **first** contact positioned over the **first surface** and coupled with the device; and a second contact positioned over the **second surface** and coupled with the device; and

(ii) a three-dimensional stacked-type package comprising: a substrate on which a number of **chips** having contacts are attached.. The **chips** are stacked with each other by the contacts and are coupled to the substrate.

USE - The direct contact through hole type wafer structure is used for forming a wafer-level package.

ADVANTAGE - Since both sides of the wafer have contacts, the **chips** can be easily stacked especially three dimensionally. Since the package is a wafer-level package and stacked three dimensionally, the volume and height of the package are decreased. Since the **chips** are coupled with other **chips** or the printed circuit board by the bumps, the signal transmitting path is reduced which leads to reduced electrical impedance. Problem of signals delaying and decaying is avoided.

pp; 15 DwgNo 0/4

67/3,AB/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013641665
WPI Acc No: 2001-125873/200114
XRAM Acc No: C01-036744
XRPX Acc No: N01-092760

Process for partially exposing a metal layer on a surface of a semiconductor **substrate** comprises **removing** a **first** part of one layer applied to the metal layer by dry etching and a second part by wet etching

Patent Assignee: SEZ SEMICONDUCTOR-EQUIP ZUBEHOER (SEZS-N); INFINEON TECHNOLOGIES AG (INFN)
Inventor: DE NIJS G; KRUWINUS H
Number of Countries: 027 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1069604	A2	20010117	EP 2000114756	A	20000710	200114	B
JP 2001068476	A	20010316	JP 2000214483	A	20000714	200121	
KR 2001069990	A	20010725	KR 200040087	A	20000713	200206	
AT 9901233	A	20011215	AT 991233	A	19990715	200208	
AT 409429	B	20020615	AT 991233	A	19990715	200248	

Priority Applications (No Type Date): AT 991233 A 19990715
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1069604	A2	G	5	H01L-021/311	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001068476	A		5	H01L-021/3205	
KR 2001069990	A			H01L-023/48	
AT 9901233	A			H01L-021/306	
AT 409429	B			H01L-021/306	Previous Publ. patent AT 9901233

Abstract (Basic): EP 1069604 A2
Abstract (Basic):

NOVELTY - Process for partially exposing a metal layer on a **surface** of a semiconductor **substrate** comprises **removing** at least a **first** part of one layer applied to the metal layer by dry etching and a second part by wet etching.

DETAILED DESCRIPTION - Dry etching removes more than 80, preferably more than 90% of the layer. Plasma etching is used in the dry etching step. Immersion, spray or rotation etching is used for the wet etching step.

USE - For treating semiconductor substrates having **bonding** or contact **pads** in the production of **integrated circuits**.

ADVANTAGE - The process is short and simple.

pp; 5 DwgNo 0/0

67/3,AB/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013484246
WPI Acc No: 2000-656189/200063
XRAM Acc No: C00-198595
XRPX Acc No: N00-486451
Controlling copper oxide formation on semiconductor **integrated circuits** for bonding comprises removing oxide layer and applying passivation layer and bonding by punching through passivation layer
Patent Assignee: LAM RES CORP (LAMR-N); HYMES D J (HYME-I); LI H (LIHH-I)
Inventor: HYMES D J; LI H
Number of Countries: 092 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200059029	A2	20001005	WO 2000US5787	A	20000306	200063	B
AU 200038677	A	20001016	AU 200038677	A	20000306	200106	

US 6358847	B1	20020319	US 99282596	A	19990331	200224
EP 1186022	A2	20020313	EP 2000917749	A	20000306	200225
			WO 2000US5787	A	20000306	
KR 2001108419	A	20011207	KR 2001712365	A	20010927	200236
US 20020058417	A1	20020516	US 99282596	A	19990331	200237
			US 200238980	A	20020104	
TW 454281	A	20010911	TW 2000106196	A	20000331	200242
JP 2002540631	W	20021126	JP 2000608434	A	20000306	200307
			WO 2000US5787	A	20000306	

Priority Applications (No Type Date): US 99282596 A 19990331; US 200238980 A 20020104

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200059029	A2	E	35	H01L-021/60	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200038677	A	H01L-021/60	Based on patent WO 200059029	
US 6358847	B1	H01L-021/44		
EP 1186022	A2 E	H01L-021/60	Based on patent WO 200059029	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

KR 2001108419	A	H01L-021/60		
US 20020058417	A1	H01L-021/44	Cont of application US 99282596	
TW 454281	A	H01L-021/60		
JP 2002540631	W	39 H01L-021/3205	Based on patent WO 200059029	

Abstract (Basic): WO 200059029 A2

Abstract (Basic):

NOVELTY - A cost-effective way of controlling the native oxide growth on copper pads of semiconductor **integrated circuits** comprises removing copper oxide layer and applying passivation layer within five seconds.

DETAILED DESCRIPTION - A cost-effective way of controlling the native oxide growth on copper pads of semiconductor **integrated circuits** comprises:

(a) removing an oxide layer from a wafer **surface** with a **first** liquid applied with a first brush located in a brush system;

(b) applying a passivation layer to the wafer **surface** with a **second** liquid applied with a second brush located in the brush system, the liquid having a reaction with the wafer **surface** to form the **second** layer; and

(c) applying a bond to the wafer surface by punching through the passivation layer.

INDEPENDENT CLAIMS are included for:

(1) a method for removing an oxide from a surface and applying a passivation layer to the surface within 5 seconds of the oxide removal;

(2) a method comprising applying a liquid to a brush and applying a liquid with a brush to a semiconductor wafer surface and forming a layer by the reaction between the liquid and the semiconductor wafer surface;

(3) a method comprising **removing** a **first** layer with a first liquid applied with a first brush, and applying a second layer

with a second liquid applied with a second brush, the second liquid reacting with the wafer **surface** to form the **second** layer;
and
(4) an apparatus comprising a supply line configured to apply a liquid to a brush, the brush being located over the surface of a wafer.
USE - Used for semiconductor **integrated circuits**.
ADVANTAGE - Provides a cost-effective method of controlling native oxide growth.
DESCRIPTION OF DRAWING(S) - The figure illustrates a bonded wire.
Capillary (106)
Gold or aluminum wire (101a, 101c)
Ball (104a, 104d)
Capillary tip (102,102a)
Chip's **bond pads** (105a)
Package lead (103a,103b, 103c)
pp; 35 DwgNo 1/4

67/3,AB/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013318224
WPI Acc No: 2000-490163/200043
Related WPI Acc No: 1997-535147; 1999-312272; 2001-549460; 2002-328901
XRAM Acc No: C00-147168
XRPX Acc No: N00-363714
Hermetically sealed semiconductor **chip** comprises a first coating sealing a **first surface** and a **second** coating sealing the first coating and **bond pad**(s)
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: AKRAM S; FARNWORTH W M; WOOD A G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6084288	A	20000704	US 96614178	A	19960312	200043	B
			US 97910613	A	19970813		
			US 99244733	A	19990205		

Priority Applications (No Type Date): US 96614178 A 19960312; US 97910613 A 19970813; US 99244733 A 19990205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6084288	A		15	H01L-023/544	Cont of application US 96614178
					Cont of application US 97910613
					Cont of patent US 5682065
					Cont of patent US 5903044

Abstract (Basic): US 6084288 A
Abstract (Basic):
NOVELTY - A hermetically sealed semiconductor **chip** comprises a semiconductor **chip** (12) having **first** and **second surfaces**, lateral edges and **bond pad**(s) (14); a first coating (30) covering the **first surface**; and a **second** coating (40) sealingly engaging the first coating and **bond pad**(s), and extending from the **bond pad**(s) to the lateral edges. The first coating includes a glass and ceramic material.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (a)

a semiconductor wafer comprising a substrate having two sides and street areas, semiconductor device(s), a first coating covering the first side and the device(s), a second coating covering the second side and filling the portion of the street areas, and a metal circuit(s) connected to the **bond pads**; and (b) a method of making a sealed semiconductor device comprising forming a semiconductor device(s) on the first side of the wafer, reducing the thickness of the wafer from the **second** side, **removing** a portion of the wafer from each side of the device, coating the second side of the wafer, removing a portion of the first coating on the first side of the wafer to uncover the **bond pad**(s), and applying a third coating to the **bond pad**(s).

USE - As semiconductor **chip**.

ADVANTAGE - The seal prevents an environmental attack of the semiconductor **chip**. It does not require the use of a separate package for the hermetic sealing of the **chip**, thus reduces the size of the **chip**.

DESCRIPTION OF DRAWING(S) - The figure shows a partial cross-sectional view of a fully hermetically sealed semiconductor **chip**.

Semiconductor **chip** (12)
Bond pad (14)
First coating (30)
Second coating (40)
pp; 15 DwgNo 11/12

67/3,AB/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013227185
WPI Acc No: 2000-399059/200034
Related WPI Acc No: 2002-469926
XRPX Acc No: N00-298931
Multi-**chip** module for low temperature co-fired ceramic circuit applications, has dielectric capacitive material filling via in substrates and engaging conductive material within via to define multilayer capacitor
Patent Assignee: HARRIS CORP (HARO)
Inventor: NEWTON C M; PALMER E G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6061228	A	20000509	US 9867606	A	19980428	200034	B

Priority Applications (No Type Date): US 9867606 A 19980428
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6061228	A		11	H01G-004/228	

Abstract (Basic): US 6061228 A
Abstract (Basic):

NOVELTY - Conductive materials are filled in a portion of the via (38) formed in multi-**chip** substrates (34a-34g). Dielectric capacitive material is filled in the via and engages conductive material to define multilayer capacitor. The **substrate cut** edge extends through a portion of via for exposing conductive material

to define bondable edge (46).

USE - For low temperature co-fired ceramic circuit applications.

ADVANTAGE - Eliminates need for any discrete capacitors on the **surface** of the **substrate** and allows for increased packaging density. As the discrete components are eliminated, the electrical performance is gained with close proximity of the embedded capacitor and other structures to the signal interface i.e. the bondable surface providing a **bond pad**.

DESCRIPTION OF DRAWING(S) - Figure represents schematic isometric view of the multi-**chip** module showing an embedded capacitor formed integral with the bondable edge surface forming an edge **bond pad**.

Multi-**chip** substrates (34a-34g)
Via (38)
Bondable edge (46)
pp; 11 DwgNo 2/6

67/3,AB/26 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013134218
WPI Acc No: 2000-306089/200027
XRAM Acc No: C00-093078
XRPX Acc No: N00-228914
Semiconductor device production comprises forming a resin sealed portion that seals a semiconductor **chip** with a metal substrate
Patent Assignee: SHINKO ELECTRIC IND CO LTD (SHIA); SHINKO DENKI KOGYO KK (SHIA)
Inventor: YONEMOCHI K; YONEMOCHI M
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 999587	A2	20000510	EP 99308578	A	19991029	200027	B
JP 2000150702	A	20000530	JP 98314738	A	19981105	200033	
KR 2000035207	A	20000626	KR 9948398	A	19991103	200111	
US 6204162	B1	20010320	US 99427933	A	19991027	200118	

Priority Applications (No Type Date): JP 98314738 A 19981105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 999587	A2	E	20	H01L-023/31	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000150702	A		9	H01L-023/12	
KR 2000035207	A			H01L-021/60	
US 6204162	B1			H01L-021/44	

Abstract (Basic): EP 999587 A2
Abstract (Basic):

NOVELTY - Semiconductor device production includes mounting a **chip** (10) on one side of a metal substrate (40), wire bonding (20) an electrode of the **chip** to a metal film (46) and sealing with resin (12).

DETAILED DESCRIPTION - Producing a semiconductor device comprises:
(a) forming a recess on one side of a metal substrate (40);
(b) providing a metal film, which dissolves the metal

substrate, on the inner **surface** of the recess and on the part of the substrate flush with one side of the substrate forming a **bonding pad** (42a);

(c) mounting a semiconductor **chip** (10) on the substrate;

(d) wire bonding (20) to form a **bonding pad**;

(e) sealing with resin; and

(f) dissolving and **removing** the metal **substrate** by etching, to expose the metal film formed on the inner surface of the recess.

AN ADDITIONAL CLAIM is included for the metal substrate (40) having a recess on one side.

USE - None given.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **bonding pad** on the metal substrate.

semiconductor (10)

resin (12)

wire bonding (20)

metal substrate (40)

bonding pad (42a)

metal film (46)

pp; 20 DwgNo 8b/14

67/3,AB/27 (Item 27 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012684389

WPI Acc No: 1999-490496/199941

XRPX Acc No: N00-068812

Semiconductor **chip** size package manufacturing method

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: CHO Y R; KIM S I; CHO Y; KIM S

Number of Countries: 003 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 98047801	A	19980915	KR 9666316	A	19961216	199941	B
US 6004867	A	19991221	US 97990070	A	19971212	200008	
JP 2988898	B2	19991213	JP 97346823	A	19971216	200004	
JP 10178124	A	19980630	JP 97346823	A	19971216	200006	
KR 222299	B1	19991001	KR 9666316	A	19961216	200108	

Priority Applications (No Type Date): KR 9666316 A 19961216

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 98047801	A			H01L-023/00	
US 6004867	A		10	H01L-021/30	
JP 2988898	B2		7	H01L-023/12	Previous Publ. patent JP 10178124
JP 10178124	A		8	H01L-023/12	
KR 222299	B1			H01L-023/00	

Abstract (Basic): KR 98047801 A

NOVELTY - A wafer (300) is attached to a substrate (320) with a terminal pad (324) formed on the top of a trace (322) **bonded** to input/output **pads** and a bottom which contacts a passivation layer. The top **surface** of the **substrate** is back-lapped and terminal pads are exposed. The substrate-wafer composite (390) is cut along a scribe line (316) to form packages (500).

DETAILED DESCRIPTION - The wafer comprises semiconductor **chips** (310) separated by a scribe line which are provided with input/output pads on an active surface with a passivation layer covering the active layer.

USE - For manufacturing **chip** size packages at the wafer level in the electronics industry.

ADVANTAGE - Allows a flexible arrangement of metallic bumps and facilitates connection of a highly integrated semiconductor **chip** electrically and mechanically to a main board occupying a relatively small surface area of the main board. Ensures that the terminal pads are not limited to being located over the center or the edge of a **chip** where the input/output pads are located and rather can be arranged over the entire area of **chip** to mass produce a **chip** size package at low cost. Protects the active surface of a **chip** from hostile environments and strengthens the package thereby ensuring that other conventional encapsulating methods are not required.

DESCRIPTION OF DRAWING(S) - The figure shows a step of **cutting** a **substrate**-wafer composite to provide individual packages.

Wafer 300
Semiconductor **chips** 310
Scribe line 316
Substrate 320
Traces 322
Terminal pads 324
Substrate wafer composite 390
Packages 500
Dwg.5E/5
US 6004867 A

NOVELTY - A wafer (300) is attached to a substrate (320) with a terminal pad (324) formed on the top of a trace (322) **bonded** to input/output **pads** and a bottom which contacts a passivation layer. The top **surface** of the **substrate** is back-lapped and terminal pads are exposed. The substrate-wafer composite (390) is cut along a scribe line (316) to form packages (500).

DETAILED DESCRIPTION - The wafer comprises semiconductor **chips** (310) separated by a scribe line which are provided with input/output pads on an active surface with a passivation layer covering the active layer.

USE - For manufacturing **chip** size packages at the wafer level in the electronics industry.

ADVANTAGE - Allows a flexible arrangement of metallic bumps and facilitates connection of a highly integrated semiconductor **chip** electrically and mechanically to a main board occupying a relatively small surface area of the main board. Ensures that the terminal pads are not limited to being located over the center or the edge of a **chip** where the input/output pads are located and rather can be arranged over the entire area of **chip** to mass produce a **chip** size package at low cost. Protects the active surface of a **chip** from hostile environments and strengthens the package thereby ensuring that other conventional encapsulating methods are not required.

DESCRIPTION OF DRAWING(S) - The figure shows a step of **cutting** a **substrate**-wafer composite to provide individual packages.

Wafer 300
Semiconductor **chips** 310

Scribe line 316
Substrate 320
Traces 322
Terminal pads 324
Substrate wafer composite 390
Packages 500
Dwg.5E/5

67/3,AB/28 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012661451
WPI Acc No: 1999-467556/199939
XRAM Acc No: C99-136992
XRPX Acc No: N99-349001
Tape automatic weld ball-type semiconductor package - includes **bonding**, **exposing** and developing the **substrate surface**
Patent Assignee: COMPAQ MFG CO LTD (COPQ)
Inventor: TSAI W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 358991	A	19990521	TW 97111658	A	19970814	199939	B

Priority Applications (No Type Date): TW 97111658 A 19970814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 358991	A		24	H01L-021/56	

Abstract (Basic): TW 358991 A
A tape automatic weld ball-type semiconductor package (2), includes: taking of substrate having polyimide of single-face copper; dry film first **bonding/exposure**/development on the **surface** of the **substrate**; electroplating of copper, nickel, gold and nickel as multiple plating on the surface not covered by the **first** dry film; **removal** of the **first** dry film; laser etching to the substrate polyimide film by controlling the anti-laser energy with the block of the thin copper, for forming perforated graphics not going through; bonding of the second dry film on the **substrate surface**, for protection of te surface plating; electrolysis in the holes of the polyimide film for forming of stuffed holes and electrolysis plating contacts slighting outward; **removal** of the **second** dry film; etching of the exposed thin copper between the multiple plating, making the adjacent electric plating layers separate one from the other and removal by etching the electro nickel layer on the multiple electric plating, making the electroplating be exposed; laser drilling in the center of the substrate and the desired through position, for forming the **chip** installation hole and the laser through hole on the substrate, making the installation hole formed with an exterior by multiple contact suspension arms, for welding of **chips**.

67/3,AB/29 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012481950
WPI Acc No: 1999-288058/199927
XRAM Acc No: C99-085141
XRPX Acc No: N99-215118
Thermally enhanced **integrated circuit** package with a heat sink structure
Patent Assignee: AMKOR TECHNOLOGY INC (AMKO-N); AMKOR ELECTRONICS INC (AMKO-N)
Inventor: HOFFMAN P
Number of Countries: 023 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9919907	A1	19990422	WO 98US19899	A	19981002	199927	B
US 6028354	A	20000222	US 97949585	A	19971014	200017	
EP 1025585	A1	20000809	EP 98949444	A	19981002	200039	
			WO 98US19899	A	19981002		
KR 2001031110	A	20010416	KR 2000704000	A	20000414	200163	
JP 2001520460	W	20011030	WO 98US19899	A	19981002	200202	
			JP 2000516373	A	19981002		
US 6423576	B1	20020723	US 97949585	A	19971014	200254	
			US 99460175	A	19991210		

Priority Applications (No Type Date): US 97949585 A 19971014; US 99460175 A 19991210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9919907	A1	E	33	H01L-023/31	
Designated States (National): CA JP KR SG					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6028354	A			H01L-023/12	
EP 1025585	A1	E		H01L-023/31	Based on patent WO 9919907
Designated States (Regional): DE FR GB IT NL					
KR 2001031110	A			H01L-023/433	
JP 2001520460	W		33	H01L-023/50	Based on patent WO 9919907
US 6423576	B1			H01L-021/44	Div ex application US 97949585 Div ex patent US 6028354

Abstract (Basic): WO 9919907 A1
Abstract (Basic):

NOVELTY - The heat sink structure may be a heat sink (40) separated from the device (32) and the substrate (44) by respective layers (38, 42). Alternatively the heat sink structure can be a mixture of a first component for decoupling thermal stress between the device and the substrate and a second component having a higher thermal conductivity than the first component.

DETAILED DESCRIPTION - **Integrated circuit** package (3) has a semiconductor device (32) with a heat sink (40) attached to the device inwardly of **bond pads** (38), and an electrically insulating substrate (44) attached to the side of the heat sink structure which is not attached to the device.

An INDEPENDENT CLAIM is also included for a method of making thermally enhanced packages for semiconductor devices by: (a) using a strip like tape carrying a number of electrically insulating substrates (44), each having a **first surface** with a heat sink structure (38,40,42) and electrically conductive traces (50) attached

thereto; (b) attaching semiconductor devices (32) to the heat sink; (c) connecting the traces to the **bond pads** (36) of the devices; (d) applying a cover layer to a **first surface** of the tape and to the **second surfaces** of the **substrates**; (e) applying encapsulant (56) to enclose the **bond pads** and sides of the heat sink structures; (f) removing the cover layer; (g) forming interconnect structures on portions of the traces in the apertures in the **substrates**; and (h) **cutting** the tape to separate the individual packages.

USE - In packaging **integrated circuit chips**.

ADVANTAGE - Heat sink (40) enhances heat transfer between the **integrated circuit** (32) and the substrate while adhesive layers (38,42), or the first heat sink component, decouples any differences in thermal expansion between the circuit, the heat sink and the substrate.

DESCRIPTION OF DRAWING(S) - The figure shows the package

semiconductor device (32)

bond pads (36)

heat sink structure (38,40,42)

substrate (46)

conductive traces (50)

encapsulant (56)

pp; 33 DwgNo 3/8

67/3,AB/30 (Item 30 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012373890

WPI Acc No: 1999-179997/199915

XRPX Acc No: N99-132215

Testing bare semiconductor device

Patent Assignee: HONEYWELL INC (HONE)

Inventor: CULLINAN D A; DUNAWAY T J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5874319	A	19990223	US 96651065	A	19960521	199915	B

Priority Applications (No Type Date): US 96651065 A 19960521

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5874319	A		4	H01L-021/66	

Abstract (Basic): US 5874319 A

Abstract (Basic):

NOVELTY - The method involves placing a die (26) on a reusable test substrate (12) and holding it on using a vacuum. Thin wires are then attached which hold the die to a **bond pad** (60) on the **substrate**. The vacuum is **removed** and the die is held in place by the wires. The test is performed and the wires removed.

DETAILED DESCRIPTION - The method of testing a bare semiconductor die involves providing a first semiconductor die (26). A reusable test **substrate** (12) with a **surface** receives the semiconductor die. The substrate has several **bond pads** (60) with conductive traces extending away from the surface and terminating in test connections. The surface has an aperture (22) extending to an

exterior (24). A vacuum force is applied to the aperture at the exterior. The first die is placed on the surface and is held at the surface by the vacuum force. Thin wires (28) are connected from the first die to a first location on selected **bond pads**. The first location allows space for several future connections. The vacuum force is **removed** with the **first** die being held in place by the thin wires. An electrical test is performed on the die using selected test connections. The thin wires are **removed** from the **first** die. A second semiconductor die is provided. A vacuum force is applied to the aperture at the exterior. The second die is placed on the surface. Thin wires are connected from the second die to a second location, spaced from the first location, on the selected **bond pad**.

USE - The method is used to test individual ICs before they are assembled into multi-**chip** modules.

ADVANTAGE - Allows die to be attached to testing device without contamination. The test package is reusable.

DESCRIPTION OF DRAWING(S) - The drawings show an elevation view of a semiconductor die test device and a plan view of a **bond pad**.

12 reusable test substrate
22 aperture
24 exterior of test surface
26 semiconductor die
28 thin wires
60 **bond pad**
pp; 4 DwgNo 1,3/3

67/3,AB/31 (Item 31 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011896783
WPI Acc No: 1998-313693/199828
XRAM Acc No: C98-096809
XRPX Acc No: N98-245878
Vertical **chip** interconnection production - with contact pad protection by passivation layer until final connection formation
Patent Assignee: SIEMENS AG (SIEI)
Inventor: ENGELHARDT M
Number of Countries: 021 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19702121	C1	19980618	DE 1002121	A	19970122	199828	B
WO 9833216	A1	19980730	WO 98DE25	A	19980107	199836	
TW 362262	A	19990621	TW 97119350	A	19971219	200028	

Priority Applications (No Type Date): DE 1002121 A 19970122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19702121	C1		5	H01L-021/768	
WO 9833216	A1	G		H01L-025/065	
	Designated States (National): JP KR US				
	Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE				
TW 362262	A			H01L-021/768	

Abstract (Basic): DE 19702121 C

A method of producing a vertical **chip** connection involves (a) applying a passivation layer (3a) onto a first **chip** (1, 2) to cover the upper face bearing contact **pads**; (b) **bonding** a **surface** of a **second chip** (5, 6) onto the first **chip** upper face by means of a bonding layer (4) and providing the second **chip** with openings which connect this **second chip surface** with its opposite surface in the region of the contact pads of the **first chip**; (c) locally **removing** the bonding layer material using these openings; (d) cleaning the inner surfaces of the openings with a medium, which allows subsequent adherent deposition of a dielectric, and then depositing dielectric in the openings; (e) partially removing the dielectric to leave spacer layers (8) on the vertical inner surfaces, thus forming new openings (7a); (f) locally removing the passivation layer, using the new openings (7a), to expose the contact pads; and (g) introducing electrically conductive connection material into the new openings. Preferably, the bonding layer (4) is of polyimide.

ADVANTAGE - The passivation layer covers and protects the contact pads until the final electrical connection step, thus avoiding physical or chemical alteration of the contact pads and resulting poor contact with the connection material (metal) in the openings.

Dwg.2/2

67/3,AB/32 (Item 32 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011269638
WPI Acc No: 1997-247541/199723
XRPX Acc No: N97-204050

Forming all silicon@ monolithic motion sensor **integrated** with conditioning **circuitry** - using sensing wafer with bulk micromachined sensing element and capping wafer with conditioning circuitry for sensor

Patent Assignee: DELPHI TECHNOLOGIES INC (DELP-N); DELCO ELECTRONICS CORP (DELC-N)
Inventor: CHILCOTT D W; KEARNEY M B; SCHUBERT P J; STALLER S E
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 772045	A1	19970507	EP 96202784	A	19961007	199723	B
US 5721162	A	19980224	US 95552401	A	19951103	199815	
EP 772045	B1	20001213	EP 96202784	A	19961007	200066	
DE 69611217	E	20010118	DE 611217	A	19961007	200111	
			EP 96202784	A	19961007		

Priority Applications (No Type Date): US 95552401 A 19951103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 772045	A1	E	17	G01P-015/08	
Designated States (Regional): DE FR GB					
US 5721162	A		14	H01L-021/00	
EP 772045	B1	E		G01P-015/08	
Designated States (Regional): DE FR GB					
DE 69611217	E			G01P-015/08	Based on patent EP 772045

Abstract (Basic): EP 772045 A

The method for forming a monolithic motion sensor involves providing a first semiconductor wafer of a first electrical conductivity type. A doped region of a second electrical conductivity type is formed in the surface of the wafer. A trench is selectively etched in the doped region so as to form a micromachined motion sensing element. Conditioning circuitry for the micromachined motion sensor is formed on a second semiconductor wafer. A recess is etched in the **surface** of the **second** wafer.

The second semiconductor wafer is bonded to the first such that the recess encases the trench and forms an enclosure for the micromachined motion sensor. A portion of the second wafer is disposed above **bond pads** on the **surface** of the **first**. The portion of the **second** wafer is **removed** so as to **expose** the **bond pads** on the **surface** of the **first** wafer.

USE/ADVANTAGE - Sensor and conditioning circuitry are contained within single monolithic wafer. Minimises overall size of sensor. Minimal number of processing steps required for production. Allows variation in size and shape of device. Protects sensor.

Dwg.1/19

Abstract (Equivalent): US 5721162 A

The method for forming a monolithic motion sensor involves providing a first semiconductor wafer of a first electrical conductivity type. A doped region of a second electrical conductivity type is formed in the surface of the wafer. A trench is selectively etched in the doped region so as to form a micromachined motion sensing element. Conditioning circuitry for the micromachined motion sensor is formed on a second semiconductor wafer. A recess is etched in the **surface** of the **second** wafer.

The second semiconductor wafer is bonded to the first such that the recess encases the trench and forms an enclosure for the micromachined motion sensor. A portion of the second wafer is disposed above **bond pads** on the **surface** of the **first**. The portion of the **second** wafer is **removed** so as to **expose** the **bond pads** on the **surface** of the **first** wafer.

USE/ADVANTAGE - Sensor and conditioning circuitry are contained within single monolithic wafer. Minimises overall size of sensor. Minimal number of processing steps required for production. Allows variation in size and shape of device. Protects sensor.

Dwg.1/19

67/3,AB/33 (Item 33 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010732264
WPI Acc No: 1996-229219/199623
XRAM Acc No: C96-072416
XRPX Acc No: N96-192493

Mfg. thin film probe structure with low capacitance, conductance and contact resistance - by using photoresist, forming metal connections, removing resist, electroplating, etching etc.

Patent Assignee: GWO J (GWOJ-I); SHY S (SHYS-I); TZENG F (TZEN-I)
Inventor: GWO J; SHY S; TZENG F
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 271006	A	19960221	TW 94106485	A	19940716	199623	B

Priority Applications (No Type Date): TW 94106485 A 19940716

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 271006	A		16	H01L-023/00	

Abstract (Basic): TW 271006 A

Mfr. of thin film probe comprises: using one transparent non-conductive material as **substrate**; covering **substrate** top **surface** with photoresist, and forming connecting via inside substrate, and filling with metal material; forming multi-metal connection structure on **substrate** back **surface** as interconnection mechanism for signal line, power line, earthing plate and each probe connecting line; **removing** photoresist, and covering **substrate** back **surface** with photoresist, then in sequence depositing chromium film and copper film to form stack structure of copper/chromium film in order to increase adherence between substrate and subsequent layers; electroplating one oxide or polyimide similar to thin sheet, and after mask exposing, developing and etching forming patterns of several round concave holes to define probe positions; by electroplating selectively depositing conductive metal with low hardness on copper/chromium film stack structure in the above round concave hole, and filling up the concave; by etching back making the surface of conductive metal with low hardness flat; removing oxide or polyimide and performing annealing treatment to decrease the hardness of conductive metal with low hardness so as to erase the stress generated by the contact of probe and **bonding pad**; depositing one conductive metal with high hardness, and after mask exposing, developing and etching forming signal or multiple probe head with high hardness; depositing one passivation of polyimide, and after mask exposing, developing and etching the polyimide exposing the probe only; by the above process achieving test metal probe with lower capacitance than conventional one, and thereby increasing testing reliability of product and decreasing mfg. cost of product; and **chip** carrier manufactured by applying the invention could achieve system test or burn-in effects to the unpackaged **chips** that are put on **IC** board or burn-in board.

Dwg.0/3

67/3,AB/34 (Item 34 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010379234
WPI Acc No: 1995-280548/199537
XRPX Acc No: N95-214065

Image appts. e.g. LED head, plasma head and image sensor - has single substrate mounting image array which is dynamically driven by anode and cathode driving **integrated circuit** and provides connections through wire **bonding pad** and data bus

Patent Assignee: KYOCERA CORP (KYOC)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

JP 7178960 A 19950718 JP 93346768 A 19931222 199537 B

Priority Applications (No Type Date): JP 93346768 A 19931222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7178960	A		6	B41J-002/44	

Abstract (Basic): JP 7178960 A

The appts. has an image array (2) which is arranged in the main **surface** of a **substrate** (6). The array is dynamically driven by an anode driving **IC** and a cathode driving **IC** (4) which are connected to a data bus (8) and a common electrode wiring (10) respectively.

A wire **bonding pad** (24,26) and the U-shaped data bus are connected and are arranged on either side of the image array sequence. The data bus is **cut**-off for every **two** arrays and is mutually connected through a through drilling (28) and a rear side wiring (14) of the substrate. The common electrode wiring is provided at the clearance between the data bus.

ADVANTAGE - Mounts image array, anode and cathode driving **IC** in single substrate; allows use of low-cost substrate, e.g. hard PCB; provides connection on substrate without soldering; prevents drive **IC** damage and incorrect operation, i.e. driving to off-state due to electro-magnetic noise; prevents noise emission of driving **IC** to periphery; keeps image appts. width small even if substrate width is increased.

Dwg.1/5

67/3,AB/35 (Item 35 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010271332
WPI Acc No: 1995-172587/199523
XRPX Acc No: N95-135309

Direct **chip** attach module mfg. method - drilling and plating vias at predetermined connection points on DCAM substrates provided in panel form and excising DCAM from panel

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: DOWNIE A P; GALLAGHER P; GARRITY J J; ROBERTSON B L; GALLAHER P
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2283863	A	19950517	GB 9323646	A	19931116	199523	B
EP 653905	A1	19950517	EP 94308374	A	19941114	199524	
JP 7183451	A	19950721	JP 94229720	A	19940926	199538	
US 5471368	A	19951128	US 94254342	A	19940603	199602	
US 5570505	A	19961105	US 94254342	A	19940603	199650	
			US 95455775	A	19950531		

Priority Applications (No Type Date): GB 9323646 A 19931116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2283863	A		11	H05K-001/18	
EP 653905	A1	E	3	H05K-003/40	
JP 7183451	A		5	H01L-025/04	
US 5471368	A		6	H05K-007/02	

US 5570505 A 6 H05K-003/34 Div ex application US 94254342
Div ex patent US 5471368

Abstract (Basic): GB 2283863 A

The method involves bonding one or more electronic components to a substrate carrying a printed circuit such that the component or components are in electrical contact with the printed circuit. Vias are formed through the substrate at predetermined connection points of the printed circuit, and the vias are plated with an electrically conductive material.

The printed circuit and attached components are excised from the **substrate** so as to **cut** through the vias, thereby providing an electrically conducive connection pad on the edge of the substrate.

ADVANTAGE - Enables dense packaging of components onto substrate and provides for easy visual inspection of solder connections between the circuit module and an electronic circuit to which it is attached.

Dwg.3,5/5

Abstract (Equivalent): US 5570505 A

A method of manufacturing an electronic circuit module comprising the steps of:

(a) **bonding** at **least** one electronic component to a **parent substrate** carrying **at** least **one** printed **circuit** line, such **that** at least a portion of said at least one electronic component is in electrical contact with at least a portion of said at least one printed circuit line,

(b) forming at least one hole through said parent substrate at least at one predetermined connection point, such that said at least one hole passes through at least one of said at least one printed circuit line,

(c) filling said at least one hole with at least one electrically conductive material, and

(d) removing a portion from said parent substrate along at least a portion of said at least one electrically conductive material to form a first substrate, such that said first substrate has secured to it at least one of said attached component, and wherein at least a portion of said at least one electrically conductive material forms at least one electrically conductive connection pad along at least one edge of said first substrate, thereby forming said electronic circuit module.

Dwg.3/5

US 5471368 A

An electronic circuit module comprising: a substrate carrying at least one printed circuit line, at least one electronic component secured to said substrate so as to be in electrical contact with said at least one printed circuit line, and wherein said substrate has at least one electrically conductive connection pad formed along at least one edge such that said at least one electrically conductive connection pad runs vertically from the top **surface** of said **substrate** to the bottom **surface** of said **substrate**.

Dwg.5/5

67/3,AB/36 (Item 36 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010156826
WPI Acc No: 1995-058078/199508
XRAM Acc No: C95-026329

XRPX Acc No: N95-045954
Manufacturing method of semiconductor device for LSI - has insulation film membrane with opening parts on top surface of **chip** through which electrodes protrude and make contact with **bonding pad**
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: EZAWA H; IDAKA T
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6338503	A	19941206	JP 93126582	A	19930528	199508	B
US 5473197	A	19951205	US 94246744	A	19940520	199603	
US 5587337	A	19961224	US 94246744	A	19940520	199706	
			US 95444513	A	19950519		
KR 138887	B1	19980601	KR 9411783	A	19940528	200015	

Priority Applications (No Type Date): JP 93126582 A 19930528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6338503	A		6	H01L-021/321	
US 5473197	A		12	H01L-021/321	
US 5587337	A		12	H01L-021/441	Div ex application US 94246744 Div ex patent US 5473197
KR 138887	B1			H01L-021/44	

Abstract (Basic): JP 6338503 A

The manufacturing method of semiconductor device involves formation of wiring on the semiconductor substrate. A common pad is present above several wirings to facilitate external electrical connection. An insulation film membrane (2) is formed on the surface of the **chip** (1). The insulation film has few opening parts. The electrodes (3) protrude from these opening parts and are connected to **bonding pad** electrically. These electrodes have a rectangular cross section.

ADVANTAGE - Minimises size of **chip**. Secures junction intensity of electrode and lead. Controls increase of occupancy area of electrode arrangement on **chip**.

Dwg.1/10

Abstract (Equivalent): US 5587337 A

Manufacturing semiconductor devices comprises: forming pad areas on a semiconductor **substrate**, forming a **passivation** film on the pad areas, and forming first openings in the passivation film in positions corresponding to the pad areas; covering the entire surface of the resulting passivation film with an organic film; forming second openings in the organic film in positions corresponding to the first openings and in communication with the respective first openings and forming groove portions in the surface of the organic film at least in positions between the second openings; effecting a heat treatment to contract the organic film and enlarge the upper end portion of the second opening in a direction towards a portion in which the groove portion is not formed; forming bump electrodes of metal connected to the pad areas in the first and **second** openings; and **removing** the organic film.

Dwg.3a/12

US 5473197 A

A semiconductor device comprising:

a plurality of pad areas formed on a semiconductor substrate, said semiconductor **substrate** having an element **region** in which a circuit pattern is formed and said pad areas being arranged along the

periphery of said element region and connected to said element region; and

a plurality of bump electrodes connected to said pad areas, each of said bump electrodes having a square bottom surface and a rectangular upper surface larger than the bottom **surface**, a shorter **one** of the sides of the upper surface having substantially the same length as one side of the square bottom surface and the cross section of each of said bump electrodes in a direction perpendicular to the periphery of said element region having a substantially trapezoidal shape.

Dwg.4,5/12

67/3,AB/37 (Item 37 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010105840
WPI Acc No: 1995-007093/199501
Related WPI Acc No: 1997-489910
XRPX Acc No: N95-005734

Multi-**chip** module packaging and interconnection structure for **integrated circuit** - forms cavities to hold die, and **bonds** die **pads** to I-O **pads** using thermo-sonic **bonding**

Patent Assignee: MICROMODULE SYSTEMS INC (MICR-N); MICROMODULE SYSTEMS (MICR-N)
Inventor: GRISWOLD B L; HO C W; ROBINETTE W C
Number of Countries: 018 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9427318	A1	19941124	WO 94US5172	A	19940510	199501	B
US 5422514	A	19950606	US 9360406	A	19930511	199528	
US 5998859	A	19991207	US 9360406	A	19930511	200004	
			US 95420844	A	19950410		

Priority Applications (No Type Date): US 9360406 A 19930511; US 95420844 A 19950410
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9427318	A1	E	34	H01L-023/02	
Designated States (National): DE GB JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5998859	A			H01L-023/02	Cont of application US 9360406 Cont of patent US 5422514
US 5422514	A		14	H05K-003/34	

Abstract (Basic): WO 9427318 A

The packaging structure includes a thin film multilayer interconnect circuit on a baseplate. The baseplate includes a **chip** mounting cavity. The circuit has one layer including several **bonding pads** on **one surface**, a **second** layer including several other **bonding pads** on a **second surface**, and a routing layer which includes several routing conductors. An **integrated circuit** dia. within the cavity has several input-output pads in contact with the **first surface** of the interconnect circuit.

The die is aligned so as to mate the input-output pads with the

first set of bending pads. The **pads** are thermo-sonically **bonded**. A layer of encapsulant is placed over the die.

ADVANTAGE - Improved contact due to reduced oxide build up. Reduced package size due to composite structure.

Dwg.2d/5

Abstract (Equivalent): US 5422514 A

The underside of a decal interconnect structure is provided with metal pads for attachment to aluminum or gold I/O pads on **one surface** of the **integrated circuit** die. A thermosonic bonding system is used to **bond** the die **pads** to the pads. The aluminum wafer is selectively **removed** forming **one** or more cavities to hold one or more die to be mounted on the MCM structure.

The die are oriented with their pads in contact with contact pads on the thin-film decal interconnect to which they are bonded and the cavities are filled with a liquid encapsulant and cured. The composite structure may be lapped down to minimize overall package thickness and to expose the backsides of the **integrated circuit** die for thermal management.

ADVANTAGE - Provides greater die packaging density because inter-die spacings are small and both sides of interconnect circuitry can be used for components and connectors.

Dwg.3/5

67/3,AB/38 (Item 38 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009996658
WPI Acc No: 1994-264369/199432
XRPX Acc No: N94-207956

Circuit assembly fabrication method esp. for multilayered three-dimensional **integrated circuit** - forming vertical feedthroughs in SOI **IC** to underlying insulator, bonding temporary **substrate** to wafer upper **surface**, thinning SOI wafer to insulator, and forming bump **bonding pads** for top and bottom interconnects

Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: FINNILA R M
Number of Countries: 018 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9417553	A1	19940804	WO 94US363	A	19940110	199432	B
EP 631692	A1	19950104	EP 94906589	A	19940110	199506	
			WO 94US363	A	19940110		
US 5426072	A	19950620	US 936601	A	19930121	199530	
JP 7506936	W	19950727	JP 94517067	A	19940110	199538	
			WO 94US363	A	19940110		

Priority Applications (No Type Date): US 936601 A 19930121
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9417553	A1	E	34	H01L-025/065	

Designated States (National): JP
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

EP 631692	A1	E	2	H01L-025/065	Based on patent WO 9417553

Designated States (Regional): FR GB

US 5426072 A 12 H01L-021/283
JP 7506936 W 11 H01L-027/00 Based on patent WO 9417553

Abstract (Basic): WO 9417553 A

The circuit fabrication process involves processing a multilayered wafer with a semiconductor material layer over a dielectric layer on a silicon **substrate surface**, to form **one** or more feedthrough conductors and circuitry within the semiconductor layer. The feedthroughs may be thick film or thin film. An interconnect is formed over the semiconductor layer, connected to the feedthrough(s). A temporary substrate is attached to the assembly, on the interconnect and opposite the semiconductor layer.

The silicon **substrate** is **removed**, by etching e.g. either in a KOH soln. or by plasma etching, to expose the dielectric layer. Pref. an etch protective material is used at the multilayered wafer edge. Additional interconnect is formed through the dielectric, for coupling to the feedthrough(s). The interconnects are pref. formed with an or solder indium bump aligned and connected to the feedthrough(s). The temporary **substrate** may be **removed** and **two** similar assemblies stacked, with interconnection through respective bumps.

USE/ADVANTAGE - In wafer stack or sawn into die after stacking. Supports bipolar, MOS and combined technologies; high circuit density with small vertical feedthrough.

Dwg.5/10

Abstract (Equivalent): US 5426072 A

A method of mfg. integrated three-dimensional i.c's involves initially providing a first and a second silicon-on-insulator (SOI) wafer, wherein each SOI wafer includes a silicon layer separated from a bulk silicon substrate by a layer of dielectric material, typically SiO2. Next, at least one electrical feedthrough is formed in each of the silicon layers and active and passive devices are formed in each of the thin silicon layers. Then interconnects are formed that overlie the silicon layer and are electrically coupled to the feedthrough. One of the wafers is then attached to a temporary substrate, such that the interconnects are interposed between the thin silicon layer and the temporary substrate.

The bulk silicon substrate of the wafer having the temporary substrate is then etched to expose the dielectric layer. Further interconnects are then formed through the exposed dielectric layer for electrically contacting the at least one feedthrough. This results in the formation of a first circuit assembly. A next step then couples the further interconnects of the circuit assembly to the interconnects of the second SOI wafer, the second SOI wafer having a bulk substrate, a dielectric layer overlying a **surface** of the **substrate**, and a layer of processed silicon overlying the dielectric layer. The temporary **substrate** is then **removed**. Additional circuit assemblies may then be stacked and interconnected to form a three-dimensional **integrated circuit**.

USE/ADVANTAGE - **Integrated circuit** mfg. technology. Small volume i.c's providing three-dimensional circuits that support MOS, bipolar, or combination technologies.

Dwg.5,6/10

67/3,AB/39 (Item 39 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009580739
WPI Acc No: 1993-274285/199335
XRPX Acc No: N93-210635
Wirebond removal appts. for semiconductor **chips** on packaging substrates - uses number of output nozzles to remove members projecting from **substrate surface** by alternating direction of fluid flow over members
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: HERNANDEZ B; HORTON R R; NOYAN I C; PALMER M J; RITTER M B
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 557771	A1	19930901	EP 93101905	A	19930208	199335	B
US 5263620	A	19931123	US 92843693	A	19920228	199348	
JP 5291363	A	19931105	JP 92341782	A	19921222	199349	
EP 557771	B1	19950705	EP 93101905	A	19930208	199531	
DE 69300229	E	19950810	DE 600229	A	19930208	199537	
			EP 93101905	A	19930208		

Priority Applications (No Type Date): US 92843693 A 19920228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 557771	A1	E	16	H05K-013/04	
Designated States (Regional): DE FR GB					
US 5263620	A		16	B26F-003/00	
EP 557771	B1	E	18	H05K-013/04	
Designated States (Regional): DE FR GB					
DE 69300229	E			H05K-013/04	Based on patent EP 557771
JP 5291363	A			H01L-021/60	

Abstract (Basic): EP 557771 A

The apparatus includes a fluid input and a number of fluid output nozzles. A manifold plate (44) directs the fluid to preselected members of the fluid output nozzles. The fluid is directed to flow in a manner to move wires (4) bonded between contact locations on an electronic workpiece (8).

The wires (4) are moved in a back and forth motion which causes the wires to break away from the contact locations.

USE/ADVANTAGE - In microelectronics industry. Reliably and cost effectively removes wires bonded between contact locations and removes large numbers of wires simultaneously so that a **chip** can be **removed** from a **substrate** in a short period of time.

Dwg.2/11

Abstract (Equivalent): EP 557771 B

An apparatus for removing a plurality of wires (4) each bonded between a first contact location and a second contact location on an electronic workpiece (8) using a fluid comprising: a fluid input (24,26; 64, 66); a plurality of fluid output nozzles (30,32;136,138,140,142); a means (44,52,56,58,60,62) for directing said fluid to preselected members of said plurality of output nozzles so that said fluid is directed to flow in a manner to move said plurality of wires in a back and forth motion which causes said plurality of wires to break away from said first and said second contact locations.

Dwg.1/10

Abstract (Equivalent): US 5263620 A

The appts. uses a fluid flow which is preferably air. A nozzle

having a number of air jets within a **chip** accommodating cavity is disposed over the **chip** to enclose the **chip** contact pads, the substrate contact **pads** and the wires **bonded** between them. Air is forced through the number of jets to cause an alternating clockwise and counter clockwise air flow which bends the number of wires back and forth until they fatigue at the contact points to the **chip** contact pads in a substrate contact pads which results in the wires being simultaneously severed from them.

The nozzle has an aperture out through which the air escapes carrying the severed wires therewith for collection in a filter.

USE - For removing wires **bonded** between **chip** contact **pads** and substrate contact pads using an alternating fluid flow.

Dwg.1/10

67/3,AB/40 (Item 40 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009490208
WPI Acc No: 1993-183743/199323
XRPX Acc No: N93-141204

Semiconductor wafer structure forming peripheral structure of semiconductor device **chip** - has insulating layer on **surface** of **substrate** with mutually insulated openings which respectively surround device areas on substrate

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI ELECTRIC KK (MITQ); MITSUBISHI ELECTRIC MACHINERY (MITQ)
Inventor: IWASAKI M; TSUKAMOTO K
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4239457	A1	19930603	DE 4239457	A	19921124	199323	B
JP 5152433	A	19930618	JP 91312257	A	19911127	199329	
TW 222711	A	19940421	TW 92101341	A	19920224	199422	
DE 4239457	C2	19950406	DE 4239457	A	19921124	199518	
IT 1255960	B	19951117	IT 92MI2707	A	19921126	199619	
KR 9616772	B1	19961220	KR 9221590	A	19921117	199931	
US 5945716	A	19990831	US 92971041	A	19921103	199942	
US 6211070	B1	20010403	US 92971041	A	19921103	200120	
			US 99329494	A	19990610		

Priority Applications (No Type Date): JP 91312257 A 19911127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4239457	A1		44	H01L-027/04	
JP 5152433	A			H01L-021/78	
TW 222711	A			H01L-021/331	
DE 4239457	C2		7	H01L-027/04	
IT 1255960	B			H01L-000/00	
KR 9616772	B1			H01L-021/78	
US 5945716	A			H01L-029/76	
US 6211070	B1			H01L-021/4763	Div ex application US 92971041

Abstract (Basic): DE 4239457 A

A semiconductor wafer structure includes a semiconductor substrate (2) with a number of semiconductor device areas (60) and a number of

cutting line areas (50) which separate the device areas from each other.

An insulating layer (7) of a first material is formed on a **surface** of the **substrate**. The isolation layer contains a number of openings (51) which each surround a respective device area, and which are electrically isolated from each other. The openings are filled with a layer of a second material which is enclosed within each opening.

ADVANTAGE - Extends life of **substrate cutting** blade. Prevents short circuits between **bonding-pads** due to cutting wafer into **chips**, and improves reliability.

Dwg.5/58

67/3,AB/41 (Item 41 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009108303
WPI Acc No: 1992-235733/199229
Related WPI Acc No: 1993-038421; 1993-169023; 1993-169053
XRAM Acc No: C92-106284
XRPX Acc No: N92-179485
Multilayer wiring board - consists of bonded blocks, each consisting of wiring layers interlaminated with polyimide layers
Patent Assignee: NEC CORP (NIDE); NITTO DENKO CORP (NITL)
Inventor: HASEGAWA S; ISHIDA H; KIMBARA K; YOKOKAWA S
Number of Countries: 006 Number of Patents: 021
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 494668	A2	19920715	EP 92100269	A	19920109	199229	B
CA 2059020	A	19920710	CA 2059020	A	19920108	199239	
JP 4312998	A	19921104	JP 9111704	A	19910109	199251	
JP 4312999	A	19921104	JP 9111705	A	19910109	199251	
JP 5037159	A	19930212	JP 91208793	A	19910726	199311	
CA 2074648	A	19930127	CA 2074648	A	19920724	199315	
JP 5144973	A	19930611	JP 91304755	A	19911120	199328	
JP 5144974	A	19930611	JP 91305943	A	19911121	199328	
CA 2083072	A	19930522	CA 2083072	A	19921117	199332	
CA 2083077	A	19930519	CA 2083077	A	19921117	199332	
JP 5206643	A	19930813	JP 91301430	A	19911118	199337	
US 5321210	A	19940614	US 92818529	A	19920109	199423	
US 5322593	A	19940621	US 92979795	A	19921120	199424	
US 5426849	A	19950627	US 92818529	A	19920109	199531	
			US 9370923	A	19930728		
EP 494668	A3	19941019	EP 92100269	A	19920109	199534	
US 5628852	A	19970513	US 92918594	A	19920724	199725	
			US 94328950	A	19941025		
EP 494668	B1	19971229	EP 92100269	A	19920109	199805	
CA 2083077	C	19971223	CA 2083077	A	19921117	199811	
DE 69223657	E	19980205	DE 623657	A	19920109	199811	
			EP 92100269	A	19920109		
CA 2059020	C	19980818	CA 2059020	A	19920108	199844	
CA 2074648	C	19990223	CA 2074648	A	19920724	199919	

Priority Applications (No Type Date): JP 91305943 A 19911121; JP 9111704 A 19910109; JP 9111705 A 19910109; JP 91208793 A 19910726; JP 91301430 A 19911118; JP 91304755 A 19911120; JP 91255517 A 19911002; JP 92219512 A

19920819

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 494668	A2	E	43	H05K-003/46	
Designated States (Regional): DE FR GB					
JP 4312998	A		12	H05K-003/46	
JP 4312999	A		9	H05K-003/46	
JP 5037159	A		9	H05K-003/46	
JP 5144973	A		10	H01L-023/12	
JP 5144974	A		14	H01L-023/12	
JP 5206643	A		8	H05K-003/46	
US 5321210	A		39	H05K-001/00	
US 5322593	A		38	B44C-001/22	
US 5426849	A		39	H01R-009/09	Div ex application US 92818529 Div ex patent US 5321210
US 5628852	A		35	H05K-003/34	Cont of application US 92918594
EP 494668	B1	E	47	H05K-003/46	
Designated States (Regional): DE FR GB					
DE 69223657	E			H05K-003/46	Based on patent EP 494668
CA 2059020	A			H05K-001/00	
CA 2074648	A			H05K-001/02	
CA 2083072	A			H05K-001/02	
CA 2083077	A			H05K-001/02	
EP 494668	A3			H05K-003/46	
CA 2083077	C			H05K-001/02	
CA 2059020	C			H05K-001/00	
CA 2074648	C			H05K-001/02	

Abstract (Basic): EP 494668 A

A multilayer wiring board is produced by assembling blocks in a stack. Each block consists of wiring layers interlaminated with polyimide insulating layers. The blocks are formed on a temporary **substrate** which is **removed** after the block is adhesively bonded to the stack. Electrical connections between blocks are made by wiring projections which contact solder pools.

A multilayer wiring board consists of a base block (10), on which are adhesively bonded, stacked wiring blocks (50). Base block (10) consists of ceramic substrate (12) which carries terminal pins (14) with interconnecting wiring (16). Polyimide layers (20,26,32,38) carry signalling, interconnecting, and grounding wiring (18,22,28,34), and are produced by known photolithographic and plating means. Successive polyimide layers are built up by known varnish and cure means. Wiring is terminated on the top layer (38) in gold/tin solder pools (40). A wiring block (50) is assembled in like manner on a temporary aluminium substrate and its wiring terminates on top layer (54) as metal bumps (52). Blocks (10,50) are assembled by reversing block (50) to juxtapose top layers (54,38), so that bumps (52) contact solder pools (40).

USE/ADVANTAGE - The process is quicker and has a better yield than the prior art.

Dwg.1/27

Abstract (Equivalent): EP 494668 B

A multilayer wiring board is produced by assembling blocks in a stack. Each block consists of wiring layers interlaminated with polyimide insulating layers. The blocks are formed on a temporary **substrate** which is **removed** after the block is adhesively bonded to the stack. Electrical connections between blocks are made by wiring projections which contact solder pools.

A multilayer wiring board consists of a base block (10), on which

are adhesively bonded, stacked wiring blocks (50). Base block (10) consists of ceramic substrate (12) which carries terminal pins (14) with interconnecting wiring (16). Polyimide layers (20,26,32,38) carry signalling, interconnecting, and grounding wiring (18,22,28,34), and are produced by known photolithographic and plating means. Successive polyimide layers are built up by known varnish and cure means. Wiring is terminated on the top layer (38) in gold/tin solder pools (40). A wiring block (50) is assembled in like manner on a temporary aluminium substrate and its wiring terminates on top layer (54) as metal bumps (52). Blocks (10,50) are assembled by reversing block (50) to juxtapose top layers (54,38), so that bumps (52) contact solder pools (40).

USE/ADVANTAGE - The process is quicker and has a better yield than the prior art.

Dwg.1/27c

Abstract (Equivalent): US 5686702 A

A multilayer wiring substrate having polyimide multiple wiring layers formed on an insulating substrate, characterized in that the polyimide multiple wiring layers are formed into a layered structure comprising a number of blocks, which blocks are stacked on one another, each of the blocks comprising a number of polyimide wiring layers formed on opposite sides of an insulating board including within the board a conductive layer, where electrical connection and bonding between adjacent blocks is established through an anisotropic conductive film interposed between the adjacent blocks.

Dwg.0/19

US 5628852 A

A method for manufacturing a polyimide multilayer wiring substrate comprises: a) forming a plurality of first wiring layer blocks, each of the first wiring layer blocks being formed by forming a layered structure of conductive wiring layers and polyimide layers on **two surfaces** of **one** of a ceramic board and a hard organic resin board having an internal conductive layer, each of the polyimide layers of the first wiring layer blocks being formed between two successive layers of the conductive wiring layers of the first wiring layer blocks, and by forming metal bumps in electrical contact with the conductive wiring layers on top and bottom surfaces of each of the first wiring layer blocks, the conductive wiring layers of the first wiring layer blocks being connected between the polyimide layers of the first wiring layer blocks through via holes; b) forming a second wiring layer block, by forming a layered structure of conductive wiring layers and polyimide layers on one of a ceramic board and a hard organic resin board, each of the polyimide layers of the second wiring layer block being formed between two successive layers of the conductive wiring layers of the second wiring layer block, and by forming metal bumps in electrical contact with the conductive wiring layers in the second wiring layer block on a top **surface** of the **second** wiring layer block, the conductive wiring layers of the second wiring layer block being connected between the polyimide layers of the second wiring layer block through via holes; c) interposing a first anisotropically conductive film, having conductive particles therein, between a bottom **surface** of **one** of the first wiring layer blocks and the top **surface** of the **second** wiring layer block; d) superposing the bottom **surface** of the **one** of the first wiring layer blocks onto the top **surface** of the **second** wiring layer block with the first anisotropically conductive film therebetween, the metal bumps on the bottom **surface** of the **one** of the first wiring layer blocks being aligned with the metal bumps on the top **surface** of the **second** wiring layer block; e) bonding and

electrically connecting the one of the first wiring layer blocks and the second wiring layer block by subjecting the one of the first wiring layer blocks and the second wiring layer block to pressure and heat, the bonding being achieved by adhesive force of the first anisotropically conductive film under conditions of pressure and heating, the electrical connection being formed in regions where the metal bumps of the one of the first wiring layer blocks and the metal bumps of the second wiring layer block press against the first anisotropically conductive film, crushing the conductive particles in the first anisotropically conductive film only between the metal bumps; f) interposing a second anisotropically conductive film, having conductive particles therein, between a bottom surface of another of the first wiring layer blocks and a top **surface** of the **one** of the first wiring layer blocks; g) superposing the bottom surface of the another of the first wiring layer blocks onto the top **surface** of the **one** of the first wiring layer blocks with the second anisotropically conductive film therebetween, the metal bumps on the bottom surface of the another of the first wiring layer blocks being aligned with the metal bumps on the top **surface** of the **one** of the first wiring layer blocks; h) bonding and electrically connecting the one of the first wiring layer blocks and the another of the first wiring layer blocks in a manner as recited in the step e; i) repeating the steps f, g and h a number of times to form multiple wiring layer blocks stacked on the one of the ceramic and hard organic resin board; and j) forming electrode pads for connecting a large scale **integrated** (LSI) **circuit** on a top **surface** of an uppermost **one** of the plurality of first wiring layer blocks.

Dwg.1/19

US 5426849 A

A method is provided for the prodn. of a multilayer wiring board comprising; (i) making a laminated base block with an electrically insulating substrate, a combination of a number of wiring layers and polyimide resin layers in an alternately laminated arrangement in the surface opposite from the polyimide; (ii) separately making a number of laminated temporary blocks each of temporary substrate with a combination of a number of alternating wiring and polyimide resin layers with electrical terminals on the **surface** opposite the temporary **substrate** which is a polyimide layer; (iii) bonding one of the temporary blocks to the base block such that the terminals align and interconnect; **removing** the temporary **substrate**; (v) providing electrical terminals on the **exposed** surface; (vi) **bonding** another temporary block to that laminate and connecting it electrically; and (vii) **removing** the temporary **substrate**

.

ADVANTAGE - Increased yield in less time.

Dwg.0/27

US 5321210 A

A multilayer wiring board has superposed laminated blocks (10, 50) bonded to each other and mounted on a substrate. Each block has multiple wiring and polyimide layers (54, 56) with polyimide (54, 38) forming the block faces for bonding to other blocks. Adjacent blocks are electrically connected to each other at a number of small areas of the interface.

The connections are pref. provided by solder polls (40) formed on one block and metal bumps (52) formed on the other to enter the pools. The pools are pref. formed of multilayer gold and tin plating and the bumps are gold plating. Blocks may be bonded to each other by thermosetting maleimide or thermoplastic

tetrafluoroethylene-perfluoroalkylvinylether copolymer adhesive.
USE/ADVANTAGE - Partic. for mounting LSI **chips**, can have high wiring density and be produced rapidly with high yield.
Dwg.1/27

67/3,AB/42 (Item 42 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008801095
WPI Acc No: 1991-305107/199142
XRPX Acc No: N91-233725
Fabrication of surface acoustic wave device - using interdigital electrode patterns with connections between interdigital electrodes and scribe lines
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: MIYASHITA T; SATOH Y
Number of Countries: 009 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 452105	A	19911016	EP 91303143	A	19910410	199142	B
CA 2040046	A	19911012				199201	
JP 3293808	A	19911225	JP 9095532	A	19900411	199207	
US 5243249	A	19930907	US 91683042	A	19910410	199337	
US 5325573	A	19940705	US 91683042	A	19910410	199426	
			US 9370176	A	19930602		
EP 452105	B1	19960228	EP 91303143	A	19910410	199613	
DE 69117321	E	19960404	DE 617321	A	19910410	199619	
			EP 91303143	A	19910410		
CA 2040046	C	19960709	CA 2040046	A	19910409	199638	
KR 9505177	B1	19950519	KR 915777	A	19910411	199703	

Priority Applications (No Type Date): JP 9095532 A 19900411
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 452105	A				
Designated States (Regional): DE FR GB NL SE					
US 5243249	A		13	H01L-041/08	
US 5325573	A		13	H01L-041/22	Div ex application US 91683042 Div ex patent US 5243249
EP 452105	B1	E	20	H03H-009/145	
Designated States (Regional): DE FR GB NL SE					
DE 69117321	E			H03H-009/145	Based on patent EP 452105
CA 2040046	C			H03H-009/64	
KR 9505177	B1			H03H-009/64	

Abstract (Basic): EP 452105 A
The surface-acoustic-wave device has a piezoelectric substrate giving a passage (CH) of waves at an upper surface. The inter digit electrodes (71,72) are aligned in the wave propagation direction and each has a part (EL1) connected to **bonding pads** (78) and with a number of finger electrodes (f1-fn) crossing the direction of the waves.
A second part (EL2) also with fingers (g1-gn) crosses the wave direction in parallel with the first set of fingers but in the opposite direction. An interconnection pattern (54) connects adjacent inter digit electrodes together.

USE/ADVANTAGE - For radio/portable telephones using surface acoustic wave SAW devices. Prevents sparking discharge between electrodes by neutralising the electric potentials. Improved operating characteristics with reduced physical size.

Dwg.6/9

Abstract (Equivalent): EP 452105 B

A wafer (51) containing a plurality of surface-acoustic-wave devices (52), comprising a substrate of a piezoelectric material and having an upper major surface and a lower major **surface**, said **substrate** providing a passage (CH) of surface acoustic waves propagating in a predetermined direction at the upper major **surface** of the **substrate**, each **surface**-acoustic-wave device having; a plurality of interdigital electrodes (71,72) provided on the upper major **surface** of the piezoelectric **substrate** to form a row in correspondence to the passage of surface acoustic waves such that the electrodes are aligned, as a row, in the propagating direction of the surface acoustic waves, each of said plurality of interdigital electrodes comprising a first part (EL1, El1') connected commonly to a **bonding pad** (78. 78') provided on the upper major **surface** of the **substrate** for external electric connection and having a plurality of finger electrodes (f1-fn or g1-gn) extending parallel with each other in a direction that is included in the upper major **surface** of the **substrate** and crossing the passage of the surface acoustic waves, and a second part separated from the first part and having a plurality of finger electrodes extending parallel with each other in a direction opposite to the direction of the finger electrodes of the first part, said first part and said second part being so disposed, in each interdigital electrode, that said finger electrodes of the first part and said finger electrodes of the second part are repated alternately in the propagating direction of the surface acoustic waves with an overlapping of the opposing finger electrodes when viewed in the propagating direction of the surface acoustic waves, said opposing finger electrodes defining the passage of the surface acoustic waves; an interconnection pattern (54) on the upper major **surface** of the **substrate** in correspondence to a region offset from the passage (CH) of the surface acoustic waves for connecting the second parts of adjacent interdigital electrodes with each other; said row of interdigital electrodes including a plurality of input interdigital electrodes (71) and a plurality of output interdigital electrodes (72) disposed alternately along the passage of the surface acoustic waves, said **bonding pad** (78, 78') including an input **bonding pad** (78) and an output **bonding pad** (78') both provided on the upper major **surface** of the **substrate** with a separation therebetween, said first part (El1) of the input interdigital electrodes being connected commonly to the input **bonding pad**, and said first part (El1') of the output interdigital electrodes being connected commonly to the output **bonding pad**; the wafer being characterised in that a first conductor layer (50) lies on the upper major surface (51) around a plurality of device patterns and a first conductor strip means (53) separates the substrate into a plurality of **chips** and is connected to the conductor layer (50) and in that the lower major surface and a side wall are covered by a second conductor layer (50a,50b) such that the first and second conductor layers are connected electrically to each other and in that the second conductor layer (50a,50b) is left unpatterned.

(Dwg.5/10

Abstract (Equivalent): US 5325573 A

The SAW device fabrication method involves covering an upper **surface** of a piezoelectric **substrate** with a conductor layer.

The conductor layer is patterned to form a number of interdigital electrodes, separated from each other by a conductor strip extending along a dicing line defined on the **substrate** upper **surface** for separation of the substrate into a number of **chips**. The interdigital electrode fingers are connected to each other.

The SAW devices are separated from each other by dicing along the dicing line so that the conductor strip is removed from each device. Pref. the SAW devices are separated by sawing, where the **substrate** is **cut** along the dicing line by a saw with a width larger than the conductor strip width.

ADVANTAGE - Eliminates sparking discharge between electrode fingers.

Dwg.5/10

US 5243249 A

The surface-acoustic-wave includes a substrate of piezoelectric material for the propagation of surface acoustic waves along a channel formed on an upper major **surface** of the **substrate**. Multiple interdigital electrodes on the piezoelectric **substrate** major **surface** in a row, in correspondence to the channel, are aligned in the propagating direction of the surface acoustic waves. Each of the interdigital electrodes has a first part connected to a **bonding pad** on the substrate for external electric connection and has multiple finger electrodes extending in parallel, spaced relationship with respect to each other in a direction transverse to and crossing the channel.

A second part is separated from the first part and has finger electrodes extending in parallel, spaced relationship with respect to each other and in a direction opposite to the direction of the finger electrodes of the first part and transverse to and crossing the channel. An interconnection pattern is provided on the **surface** of the **substrate** in correspondence to a region which is offset from the channel interconnecting the respective second parts of the adjacent interdigital electrodes.

ADVANTAGE - Eliminates discharge between fingers, without affecting performance.

ec

Dwg.6/10

67/3,AB/43 (Item 43 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008659709
WPI Acc No: 1991-163736/199122
XRPX Acc No: N91-125473

Large expandable array thermal ink jet pen - has print heads spaced on and secured to insulating substrate each having ink feed ports

Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: CHAN C S; HANSON G E; WRIGHT C L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5016023	A	19910514				199122	B

Priority Applications (No Type Date): US 89417936 A 19891006

Abstract (Basic): US 5016023 A

A number of individual thin film ink jet printheads, each including an orifice plate, are selectively spaced on and secured to an insulating substrate having ink food ports therein which supply ink to the printheads. Buss lines and **integrated circuit** driver-decoder packages may be mounted in a planar fashion w.r.t. the printheads and electrically interconnected to drive the printheads.

The individual printheads may be mounted on a unitary insulating support and ink feed structure such as a ceramic substrate and interconnected to off-substrate TIJ driver circuitry by way of printed or silk-screened electrical leads. These leads may be laid down in a controlled pattern on the **surface** of the ceramic **substrate** and used to interconnect **bonding pads** on the TIJ printheads with the above off-substrate driver circuitry and power supplies. If desired, **integrated circuit** packages may be mounted in slots **cut** in the ceramic **substrate** in a planar arrangement w.r.t. the printheads.

ADVANTAGE - Overcomes mismatch sandwich structures and electrical interconnect problems. (8pp Dwg.No.1/3

67/3,AB/44 (Item 44 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007984895
WPI Acc No: 1989-250007/198935
XRPX Acc No: N89-190574
Die attach pick-up tool for **IC** mfr. - has passage extending from hole through tool for connection to vacuum source
Patent Assignee: DU PONT DE NEMOURS & CO E I (DUPO)
Inventor: SAKIADIS B C
Number of Countries: 009 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 329823	A	19890830	EP 88114252	A	19880901	198935	B
JP 1235339	A	19890920	JP 88216446	A	19880901	198944	
US 4875279	A	19891024	US 88158729	A	19880222	199001	
CA 1289990	C	19911001				199146	

Priority Applications (No Type Date): US 88158729 A 19880222; US 8731793 A 19870330; US 8788141 A 19870821
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 329823	A	E	13		
Designated States (Regional): DE FR GB IT LU NL					
US 4875279	A		11		

Abstract (Basic): EP 329823 A

The die attach pickup tool is provided for picking up a flexible die attach having a **first** area from a **cutting** station, transferring the die attach to a bond site and depositing the die attach on the bond site. The tool comprises a face for contacting the die attach, the face having a **second surface** area of at least about 1.27 mm square and a hole. A passage is connected to the

hole for connecting to a vacuum source.
When each point of the **first surface** area is in contact with a point of the **second surface** area or adjacent the hole then, upon turning on the vacuum source, the tool is adapted to pickup and transfer the die attach and, upon turning the vacuum source off, the tool is adapted to deposite the die attach, all in a substantially flat position.
USE - For relocating pad of flexible ribbon for bonding **IC chips** to substrate.
2/14

Abstract (Equivalent): US 4875279 A
The tool picks up a flexible ribbon shaped die attach of thickness 25 to 125 micrometers, and an elastic modulus 500 to 7500 N/mm square at 23 degrees C. The tool has a face of area at least 1.27 mm square for contacting the die attach, the face having a hole of diameter 0.254 to 0.900 mm through which a vacuum is passed.
The die attach is picked up from a cutting station and transferred to a bond site where it is deposited, all while the die attach is in a substantially flat position.
USE - Relocates flexible die attach **pads** for **bonding integrated circuit chips** to substrates in a flat position. (11pp)

67/3,AB/45 (Item 45 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004505154
WPI Acc No: 1986-008498/198602
XRAM Acc No: C86-003560
XRPX Acc No: N86-006103
Prodn. of silicon-on-insulator structure and transistor mfr. - by bonding substrate carrying epitaxial layer and oxide layer to second substrate via oxide layer
Patent Assignee: IBM CORP (IBMC)
Inventor: ABERNATHEY J R; KINNEY W I; LASKY J B; STIFFLER S R
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 166218	A	19860102	EP 85106383	A	19850524	198602	B
JP 61014745	A	19860122	JP 8530654	A	19850220	198610	
US 4649627	A	19870317	US 84625758	A	19840628	198713	
EP 166218	B	19900328				199013	
DE 3576883	G	19900503				199019	

Priority Applications (No Type Date): US 84625758 A 19840628
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 166218	A	E	22		
Designated States (Regional): DE FR GB					
EP 166218	B	E			
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 166218 A
Bonded **IC** structures are formed by: depositing an epitaxial layer on a first side of a semiconductor substrate; forming an Si oxide layer on the epitaxial layer; bonding the structure to a second

substrate at a predetermined temp. in an oxidising atmos. using the oxide layer as bonding material; and **removing** the **first substrate** to expose the epitaxial layer.

USE/ADVANTAGE - The resulting Si-on-insulator wafer is used to form two FETs with a shared element, pref. source or drain of one and gate electrode of the other, formed in the epitaxial layer (claimed). A high degree of integration is achieved.

9/15

Abstract (Equivalent): EP 166218 B

A method of fabricating an integrated semiconductor structure, comprising at least two FETs with a shared element, the method comprising the steps of depositing an epitaxial semiconductor layer (22) on a first semiconductor substrate (20); providing a second semiconductor substrate (24); forming a silicon oxide layer (e.g. 26) of a predetermined thickness on at least **one** of the **surfaces** of said **second** semiconductor substrate (24) or of said epitaxial layer (22); bonding said second semiconductor substrate on said epitaxial layer of said first semiconductor substrate at a predetermined temperature in an oxidizing atmosphere using said silicon dioxide layer (e.g. 26) as the bonding material, thereby forming a bonded structure; **removing** said **first substrate** (20) from said **bonded** structure to **expose** a major surface of said epitaxial layer (22); removing said epitaxial layer (22) in selected areas to form **active** device **regions** of said epitaxial layer (22); forming a field oxide (38) on areas other than said **active** device **regions**; forming a gate oxide (42) and gate electrode (50) over a predetermined portion of said **active** device **regions** of said epitaxial layer; defining and forming epitaxial source and drain regions (60, 62) of an epitaxial FET (70) of a conductivity type opposite to the conductivity type of said epitaxial layer; and defining and forming source and drain regions (64, 66) of a bulk FET (68) in regions of said second semiconductor substrate (24) adjacent and on either side of at least one of said epitaxial source and drain regions (60, 62), said source and drain regions (64, 66) having a conductivity type opposite to the conductivity type of said second substrate (24), and one of said epitaxial source and drain regions (60, 62) forming the gate electrode of the bulk FET (68).

(10pp

Abstract (Equivalent): US 4649627 A

Si-on-insulator transistor structure is formed with an epitaxial layer followed by a Si oxide layer, on a substrate which is then bonded to a second substrate via the oxide layer. The **first substrate** is **removed** followed by selective areas of the epitaxial layer to form **active** device **regions**. Fields oxide is formed on areas other than **active** device **regions**. Gate oxide is formed over the **active** device **regions** and a conductive gate electrode is formed over part of the gate oxide.

SOI source and drain regions are formed in the epitaxial layer on the sides of the gate electrode. Bulk source and drain regions are formed on the sides of the SOI source and/or drain regions.

USE/ADVANTAGE - Dense **integrated circuit** with vertical layers of elements, and made with relatively few interconnects. (8pp)e

67/3,AB/46 (Item 46 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002013460
WPI Acc No: 1978-26486A/197814
Semiconductor **integrated circuit** with projection electrode - which comprises a pad, coated with a chromium and a gold layer
Patent Assignee: HAMASAYA KOGYO KK (HAMA-N); SUWA SEIKOSHA KK (SUWA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 53020858	A	19780225				197814	B

Priority Applications (No Type Date): JP 7695605 A 19760811

Abstract (Basic): JP 53020858 A
An Au projection electrode for semiconductor **integrated circuits** comprises a pad formed on an **integrated circuit** substrate, a barrier metal layer of Cr formed on the pad, and an Au layer covering the Cr layer.
After a passivation layer is formed on a semiconductor substrate, except an Al **bonding pad**, to protect Al wiring layers and semiconductor elements, a Cr barrier layer is deposited over the **substrate surface** by vacuum deposition or sputtering. An Au layer is then deposited on the barrier layer. The substrate is covered with a photoresist layer, except the Al **bonding pad**, and Au is electrolytically plated on the Au layer to make an Au projection electrode.
The photoresist layer, the Au layer and the Cr layer are selectively **removed** from the **substrate surface** by selective etching to provide an Au-Cr electrode structure.
The electrodes are of simple structure and are easily mfd. at decreased cost

67/3,AB/47 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05923105
MANUFACTURE FOR MICRO BRIDGE SENSOR

PUB. NO.: 10-206205 [JP 10206205 A]
PUBLISHED: August 07, 1998 (19980807)
INVENTOR(s): AZUMI JUNICHI
YAMAGUCHI TAKAYUKI
UENISHI MORIMASA
SATO YUKITO
SHOJI HIROYOSHI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
RICOH SEIKI CO LTD [486165] (A Japanese Company or Corporation), JP (Japan)
RICOH ELEMEX CORP [360109] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-009057 [JP 979057]
FILED: January 22, 1997 (19970122)

ABSTRACT
PROBLEM TO BE SOLVED: To form a thin film sensor part within a correct plane agreeing with a **surface** of a **substrate**, by forming the

thin film sensor part on the **surface** of the **substrate**, forming a recessed part on the **surface** of the **substrate** with leaving a bridge part where the thin film sensor part is located, filling a filler in the recessed part, **cutting** the **substrate** into a plurality of **chips**, and removing the filler.

SOLUTION: An SiO(sub 2) film 2 is formed at a rear face of a substrate 1 to prevent etching and an insulating film 3 of Ta(sub 2)O(sub 5) or the like is formed at a front face of the substrate 1. A resistor film 4 is formed thereon, and a Ta(sub 2)O(sub 5) film 5 as an etching mask is formed further. The resistor film 4 and Ta(sub 2)O(sub 5) film 5 are patterned. A passivation film is formed on the front face including heat-generating bodies 6, 7, **bonding pads** 6a, 7a and a gas temperature-measuring body. The passivation film and insulating film 3 are patterned. Accordingly, two thin film sensor parts S are formed on the front face of the silicon wafer 1. Thereafter, a recessed part 10 is formed with leaving a bridge part 11. A filler 12 is filled in the recessed part, and then the wafer is cut to **chips** 13, 14. The filler is removed last.

67/3,AB/48 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04385556
SEMICONDUCTOR DEVICE

PUB. NO.: 06-029456 [JP 6029456 A]
PUBLISHED: February 04, 1994 (19940204)
INVENTOR(s): IZAWA RYUICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-207231 [JP 92207231]
FILED: July 11, 1992 (19920711)
JOURNAL: Section: E, Section No. 1544, Vol. 18, No. 238, Pg. 143, May 06, 1994 (19940506)

ABSTRACT

PURPOSE: To promote a reduction in cost and acceleration of a computer, etc., using a multichip module technique by deleting an area of a **chip** of a multichip module and suppressing a signal delay therein while enhancing yield of a product.

CONSTITUTION: A plurality of **chips** 3 for constituting a multichip module are face up placed on a **chip** placing substrate 1a, and a circuit substrate 2a to be formed with a wiring layer 4 between **chips** for electrically connecting the **chips** 3 on its surface is so laminated on a **chip** placing **surface** of the **substrate** 1a as to be opposed to the **chip** placing surface. Further, a rear **surface** of the **substrate** 1a is connected to a predetermined heat sink, and a **bonding pad** 5a to be connected to the layer 4 between the **chips** corresponding to the rear **surface** of the **substrate** 2a through **penetrating** wiring 6 is provided on the rear **surface** of the **substrate** 2a, and connected to external terminal corresponding to the pad by LOC technique.

67/3,AB/49 (Item 3 from file: 347)

03757552
MANUFACTURE OF END FACE THERMAL HEAD

PUB. NO.: 04-122652 [JP 4122652 A]
PUBLISHED: April 23, 1992 (19920423)
INVENTOR(s): KAMEDA KOJI
KASAI IKUO
GOTO HIROYUKI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-243325 [JP 90243325]
FILED: September 12, 1990 (19900912)
JOURNAL: Section: M, Section No. 1294, Vol. 16, No. 376, Pg. 158, August 12, 1992 (19920812)

ABSTRACT

PURPOSE: To make it possible to print even on a record medium which can not be folded easily by covering protruded strips formed on the **surface** of a **substrate** with a glaze layer, forming a heating element arranged along the direction to the protruded strips, an electrode connected thereto, a protective film and **bonding pad** on the glaze layer, and **cutting** off the **substrate** at an interstice of the protruded strips so as to stick to an end face of a support plate.

CONSTITUTION: A plurality of protruded strips are formed on the **surface** of a **substrate** 2. The protruded strips are covered with a glaze layer 4. A heat element 6 arranged along the direction of the protruded strips, an electrode 12 connected thereto, a protective film 14 and a **bonding pad** 16 are formed on the glaze layer. The **substrate** is **cut** off at an interstice of the protruded strips, and then, it is stuck to an end face of a support plate 18. At this time, the heating element 6 is to be formed in a position deviated from the top position of the protruded strip in order to make it easy to make electrodes 6, 8, 10 patterned. Also, in order to make it easy to connect to a semiconductor **integrated circuit** device 22 for driving the heating element, the back face of the substrate is polished in an oblique direction such that the heating element comes to the top position of the protruded strip after the **substrate** is **cut** off.

67/3,AB/50 (Item 4 from file: 347)

03693442
CONNECTING METHOD OF **INTEGRATED CIRCUIT** ELEMENT

PUB. NO.: 04-058542 [JP 4058542 A]
PUBLISHED: February 25, 1992 (19920225)
INVENTOR(s): MATSUI KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-170961 [JP 90170961]
FILED: June 28, 1990 (19900628)
JOURNAL: Section: E, Section No. 1215, Vol. 16, No. 259, Pg. 155, June

11, 1992 (19920611)

ABSTRACT

PURPOSE: To connect and **bond** an electrode **pad** to an electrode terminal with good reproducibility and stably by a method wherein a resin layer on the electrode pad on a semiconductor element or on the surface of the electrode terminal on a **substrate** is **removed**.

CONSTITUTION: Electrode pads 2 are formed on the surface of a semiconductor **integrated circuit** element (LSI **chip**) 1; and electrode terminals 4 are formed on a substrate 3 so as to correspond to the electrode pads 2. The **surface** of the **substrate** 3 is coated uniformly with a photosensitive and thermoset resin 5 by using a spinner or the like. After the resin dried, it is irradiated with ultraviolet rays 7 by using a photomask 6. A developing operation is executed. The resin on the electrode terminals 4 is removed. Then, the LSI **chip** 1 is placed on the substrate 3; the electrode pads 2 are faced with the electrode terminals 4; a load of about 10kg/cm(sup 2) is applied; this assembly is heated up to about 250 deg.C; the resin 5 is hardened; and the **chip** 1 is fixed and bonded to the substrate 3. Thereby, a high-density connecting operation can surely and easily be executed.

67/3,AB/51 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03348742
SUPERCONDUCTIVE **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 03-011642 [JP 3011642 A]
PUBLISHED: January 18, 1991 (19910118)
INVENTOR(s): AOYANAGI MASAHIRO
APPLICANT(s): AGENCY OF IND SCIENCE & TECHNOL [000114] (A Japanese Government or Municipal Agency), JP (Japan)
APPL. NO.: 01-146279 [JP 89146279]
FILED: June 08, 1989 (19890608)
JOURNAL: Section: E, Section No. 1050, Vol. 15, No. 125, Pg. 10, March 27, 1991 (19910327)

ABSTRACT

PURPOSE: To prevent a **bonding pad** from being exfoliated by a method wherein a binding member whose rear surface is connected to a substrate and which is composed of a superconducting material is formed in a through hole made in an insulating film and the **bonding pad** which is composed of the superconducting material is connected to the surface of the binding member.

CONSTITUTION: An Si wafer is used as a substrate 1; Nb or NbN is used as a material for an interconnection 4; Nb or NbN is used as a pillar-shaped binding member 5. An insulating film 2 which is situated under a **bonding pad** 3 and just above the **substrate** 1 is **removed**; a through hole is made. The binding member 5 is situated in the through hole; its rear surface is brought into a close contact with the **substrate** 1 and its **surface** is brought into a close contact with the **bonding pad** 3. Thereby, even when the insulating film is not brought into close contact with the interconnection satisfactorily, it is possible to prevent the **bonding pad** from being exfoliated.

67/3,AB/52 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01813542
MANUFACTURE OF HYBRID **INTEGRATED CIRCUIT**

PUB. NO.: 61-027642 [JP 61027642 A]
PUBLISHED: February 07, 1986 (19860207)
INVENTOR(s): SUZUKI KOHEI
SHIMADA OSAMU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-147612 [JP 84147612]
FILED: July 18, 1984 (19840718)
JOURNAL: Section: E, Section No. 414, Vol. 10, No. 179, Pg. 52, June 24, 1986 (19860624)

ABSTRACT

PURPOSE: To facilitate an exchange of defective **chips** and to uphold the manufacturing yield of a hybrid **integrated circuit** by a method wherein a defective element in the defective **region** of the **substrate** is **removed**, a new **second substrate**, whereon the same wiring pattern as that in the circumferencial region of the defective element is performed, and a new element are mounted on the defective region and the new second substrate and the substrate are electrically connected.

CONSTITUTION: A defective element 2' in a defective region 4', wherein there exist the defective element 2' and a defective wiring pattern, is **removed**, a **substrate** 5, whereon the same wiring pattern as that in the defective region 4' is performed, is bonded on the region 4' and a new element 2'' is mounted. After that, an electric connection between the substrate 1 and the wiring pattern on the substrate 5 is performed using a connecting means, such as bonding wires 6. By this way, even when there exists a damage, which is not correctable, in the wiring and the **bonding pad** in the defective region, the whole defective region is exchanged with a new one and the hybrid **integrated circuit** can be easily turned into a non-defective one.

67/3,AB/53 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01739149
INTEGRATED CIRCUIT DEVICE

PUB. NO.: 60-217649 [JP 60217649 A]
PUBLISHED: October 31, 1985 (19851031)
INVENTOR(s): KOBAYASHI KENJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-073814 [JP 8473814]
FILED: April 12, 1984 (19840412)
JOURNAL: Section: E, Section No. 388, Vol. 10, No. 65, Pg. 159, March

14, 1986 (19860314)

ABSTRACT

PURPOSE: To improve both heat dissipating efficiency and terminal density as well as to contrive miniaturization of the titled device by a method wherein an external connection terminal pad is arranged at the bottom face of a substrate, and a structure wherein an **IC chip** main body is bonded on the cover side is obtained.

CONSTITUTION: The **bonding pads** 12 of the same number as **IC** terminals are formed on the **surface** of a **substrate** 7, and the **IC** lead 11 of an **IC chip** 8 is connected by **bonding** to each **bonding pad** . Also, a plurality of connection wiring formed on the **surface** of the **substrate** 7 are connected to the **bonding pad** 12, and besides, each of the connection wirings 17 is connected to the terminal pads 10 formed on the reverse side of the substrate 7 through the viahol wiring 16 formed in the substrate 7. The **bonding pad** 12 is connected to the viahol wiring 16 through the intermediary of the connection wiring 17, and besides, each of the viahol 16 is connected to terminal pads 10 respectively **penetrating** the **substrate** 7.

67/3,AB/54 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01415058
HYBRID **INTEGRATED CIRCUIT**

PUB. NO.: 59-126658 [JP 59126658 A]
PUBLISHED: July 21, 1984 (19840721)
INVENTOR(s): HAYASHI TETSUO
OSATO MASATOSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-001851 [JP 831851]
FILED: January 10, 1983 (19830110)
JOURNAL: Section: E, Section No. 279, Vol. 08, No. 250, Pg. 93, November 16, 1984 (19841116)

ABSTRACT

PURPOSE: To previously perform the test for evaluating **IC chips** and facilitate the exchange of defective **IC chips** after mounting by adhesion-fixing electrode patterns of the first and second substrate after the first substrate loaded with an **IC chip** is combined with the second substrate wherein it can be fitted.
CONSTITUTION: After fusing the **IC chip** 3 to the first substrate 7 by means of solder, the **bonding pads** of the **IC chip** 3 are connected to the electrode wiring pattern 8 by means of bonding wires 4. The test for the **IC chip** 3 is performed at this step. Non-defectives whose reliability is ensured are opposed to each other so that the surface for loading the **IC chip** 3 of the first **substrate** 7 contact the **surface** whereon the electrode wiring pattern 2 of the second substrate 2 is laid, and so that the **IC chip** 3 may come in the right position of a relief hole 9, thus electrically connecting the corresponding electrode wiring patterns 8 and 2 of both the substrates by a method such as soldering. If there are

IC chips judged as defective in the test for the entire body after completing a hybrid **IC**, the **first substrate** thereof is **removed** by fusing again the solder and then exchanged.

67/3,AB/55 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

00647722
MANUFACTURE OF THIN-FILM MAGNETIC HEAD

PUB. NO.: 55-135322 [JP 55135322 A]
PUBLISHED: October 22, 1980 (19801022)
INVENTOR(s): YONEOKA SEIJI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-043012 [JP 7943012]
FILED: April 11, 1979 (19790411)
JOURNAL: Section: P, Section No. 44, Vol. 05, No. 5, Pg. 3, January 14, 1981 (19810114)

ABSTRACT

PURPOSE: To improve the efficiency of the slider work of a magnetic head by combining etching with mechanical work when **cutting** a **substrate**, which has **chips** formed of a slider part and horizontal magnetic head, into individual **chips**.

CONSTITUTION: At a fixed position on the **surface** of **substrate** 6, thin-film horizontal magnetic head 7 is formed and on it, photoresist 8 is **bonded**, **exposed** via photomask 9 with a pattern for the formation of a cut position and slider and processed, thereby removing photoresist 8 at groove formation part 10. Next, groove 11 is made in substrate 6 by etching and after remaining photoresist 8 is **removed**, **substrate** 6 is separated into respective **chips** by cutting along groove 11 as shown the chain lines through mechanical work. Here, the above-mentioned mechanical work never influences the area of a slider floating surface even if its position would shifts a little, so that the slider can be formed through relatively-rough work.

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  28aug03 10:04:56 User267149 Session D951.1

File 342:Derwent Patents Citation Indx  1978-01/200330
       (c) 2003 Thomson Derwent
*File 342: Updates 200160-200209 replaced. See HELP NEWS 342.
Alert feature enhanced for multiple files, etc. See HELP ALERT.
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CITATION

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SYSTEM:OS  - DIALOG OneSearch
  File 347:JAPIO  Oct 1976-2003/Apr(Updated 030804)
         (c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 350:Derwent WPIX  1963-2003/UD,UM &UP=200355
         (c) 2003  Thomson Derwent

Set     Items   Description
S1        126   S1:S18
S2          2   S1 AND PLANAR???????(3N)INDUCT??????
S3        124   S1 NOT S2
S4         46   S3 AND ((INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?))
               OR IC OR CHIP? ?)
S5          2   S4 AND SUBSTRATE? ?(3N)(PASSIV???????? OR ACTIV????????)
S6         44   S4 NOT S5
S7          4   S6 AND SCRIB???????(3N)LINE? ?
S8         40   S6 NOT S7
S9          0   S8 AND (ALIGN???????? OR ARRANG?????? OR PARALLEL????? OR -
              GLASS OR CUTTING OR CUT)(3N)SCRIB??????
S10         0   S8 AND CONDUCT???????(3N)INTERCONNECT???????
S11         5   S8 AND BOND????????(3N)PAD? ?
S12         5   IDPAT (sorted in duplicate/non-duplicate order)
S13        35   S8 NOT S12
S14         0   S13 AND EXPOS????????(3N)BOND???????
S15         0   S13 AND (CUTTING OR CUT OR SLICE???? OR INCISE???? OR REMO-
              V??????? OR PENETRAT??????)(3N)SUBSTRATE? ?
S16         0   S13 AND (CUTTING OR CUT OR SLICE???? OR INCISE???? OR PENE-
              TRAT?????????)(3N)(PARTIAL??????? OR INCOMPLETE????????)
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2/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008908330
WPI Acc No: 1992-035599/**199205**
XRAM Acc No: C92-015520
XRPX Acc No: N92-027113
Planar inductor mfr. - by laminating film coil on high permeability alloy band via insulator and cutting resultant laminate to length NoAbstract Dwg 1/2
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3280512	A	19911211	JP 9081861	A	19900329	199205	B

Priority Applications (No Type Date): JP 9081861 A 19900329

2/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007836569
WPI Acc No: 1989-101681/**198914**
XRPX Acc No: N89-077566
Planar inductor for output choke of DC-DC converter - has spiral coils to give opposite current flow arranged in layers and side-by-side between ferromagnetic ribbons
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: HASEGAWA M; SAHASHI M
Number of Countries: 005 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 310396	A	19890405	EP 88309056	A	19880929	198914	B
JP 1157507	A	19890620	JP 8862261	A	19880316	198930	
JP 1157508	A	19890620	JP 8862262	A	19880316	198930	
JP 1310518	A	19891214	JP 88142043	A	19880609	199005	
JP 1318212	A	19891222				199006	
US 4959631	A	19900925	US 88250401	A	19880928	199041	
EP 310396	B1	19950719	EP 88309056	A	19880929	199533	
DE 3854177	G	19950824	DE 3854177	A	19880929	199539	
			EP 88309056	A	19880929		

Priority Applications (No Type Date): JP 88151779 A 19880620; JP 87245472 A 19870929; JP 87245473 A 19870929; JP 8862261 A 19880316; JP 8862262 A 19880316; JP 88142043 A 19880609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 310396	A	E	3		
Designated States (Regional): DE FR GB					
EP 310396	B1	E	34	H01F-005/00	
Designated States (Regional): DE FR GB					
DE 3854177	G			H01F-005/00	Based on patent EP 310396

Abstract (Basic): EP 310396 A
Two pairs of spiral conductor coils (1a, 1b, 1a', 1b') of the same shape, each arranged in two layers, flush with and close to each other, have insulating layers (3a, 3b, 3c) between them, Multiple layers of high-permeability amorphous alloy ferromagnetic ribbons (2a, 2b) of area greater than that of the coils are bonded on either side of the assembly on the insulating layers (3a, 3c). The conductor coils are connected electrically so that currents flow in opposite directions through each two adjacent coils.
USE/ADVANTAGE - Output choke coil of DC-DC converter, Inductance per unit volume is good in small thickness. Good DC superposition characteristic.
1,2/28
Abstract (Equivalent): EP 310396 B
A **planar inductor** comprising spiral conductor coil means (5a,5b) sandwiched between ferromagnetic layers (2a,2b) with insulating layers interposed therebetween, characterised in that each said ferromagnetic layer includes a plurality of ferromagnetic sheets each having a thickness of 100 micrometer or less.
Dwg.1a/28
Abstract (Equivalent): US 4959631 A

A **planar inductor** has a spiral conductor coil sandwiched between ferromagnetic layers with insulating layers interposed between. The spiral conductor coil means is formed of two spiral conductor coils of the same shape arranged flush with and close to each other. Moreover, the two spiral conductor coils are connected electrically to each other so that currents of different directions flow individually through the conductor coils.

The spiral conductor coil is sandwiched between the two ferromagnetic layers with the insulating layers between. Each of the ferromagnetic layers has an area greater than the combined area of the two conductor coils.

ADVANTAGE - Inductance is prevented from lowering while its components are being bonded together, so that inductance value per unit volume is increased. (32pp

5/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009423300
WPI Acc No: 1993-116815/**199314**
XRPX Acc No: N93-089083
Semiconductor wafer scribing and dicing method - masking active areas, with scribe channels exposed and etched to form V-shaped grooves for die separation
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: BEAN K E; FREEMAN J W; MCGRATH R D; POWELL J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5196378	A	19930323	US 87134398	A	19871217	199314 B
			US 89363314	A	19890605	
			US 90550234	A	19900710	
			US 91679122	A	19910325	

Priority Applications (No Type Date): US 87134398 A 19871217; US 89363314 A 19890605; US 90550234 A 19900710; US 91679122 A 19910325
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5196378	A		8	H01L-021/00	Cont of application US 87134398 Cont of application US 89363314 Div ex application US 90550234

Abstract (Basic): US 5196378 A

The method involves forming **integrated circuit** dice on a wafer with an electrically **active** layer overlying a **substrate**, where a silicon semiconductor wafer having **integrated circuit** dice with corners, is oriented so that the wafer represents a (100) orientation silicon crystal. A mask is applied to a surface of the wafer which covers active regions of the dice and has an opening along an edge of each dice, forming a straight line between adjacent corners of each dice.

The mask opening is aligned in a <110> direction of the wafer. The wafer is anisotropically etched through the active layer and into the substrate layer through the opening to form a generally V-shaped channel in the two layers. Adjacent dice are separated along a vertex of the channel.

ADVANTAGE - Allows active circuit areas as near as possible to scribe areas. Minimal die edge damage.

Dwg.6/6

5/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008286201
WPI Acc No: 1990-173202/**199023**
XRAM Acc No: C90-075417
XRPX Acc No: N90-134692
Mfg. high density, buried metal layer semiconductor structure - by forming oxide bond between two metal layers
Patent Assignee: MCNC (MCNC-N); MICROELTRN N CAROLI (MICR-N); NORTHERN TELECOM LTD (NELE); MCNC RES TRIANGLE PARK (MCNC-N)
Inventor: REISMAN A; TURLIK I; NAYAK D
Number of Countries: 016 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 371861	A	19900606	EP 89403264	A	19891127	199023	B
CA 2004075	A	19900529				199033	
JP 2199860	A	19900808	JP 89306745	A	19891128	199038	
US 5025304	A	19910618	US 88277607	A	19881129	199127	
US 5168078	A	19921201	US 88277607	A	19881129	199251	
			US 90631671	A	19901221		

Priority Applications (No Type Date): US 88277607 A 19881129; US 90631671 A 19901221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 371861	A				
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 5168078	A		8	H01L-021/3205	Div ex application US 88277607 Div ex patent US 5025304

Abstract (Basic): EP 371861 A

Mfr. involves (1) providing a first semiconductor substrate; (2) providing a second substrate; (3) forming at least one metal layer on at least one of the first and second substrates; (4) placing the two substrates against each other with the metal layer in between, and (5) heating in a oxidising atmos. to bond the two substrates, forming a buried metal layer semiconductor device.

USE/ADVANTAGE - Used to mfr. semiconductor wafers for very large scale and ultra large scale integration **chips**, permiting the formation of high density interconnection patterns and maintaining a high level of device isolation. (7pp Dwg.No.1B/29)

Abstract (Equivalent): US 5168078 A

A semiconductor (SC) device is produced by (A) forming at least 1 metal layer on (a) a 1st SC substrate (S) and on (b) a 2nd SCS, (B) placing the 1st SCS onto the 2nd SCS with at least 1 metal layer being between them and (C) bonding the 1st SCS to the 2nd SCS by heating them in an oxidising ambient atmos. to form a buried metal layer SC device. An insulating layer is pref. formed on the 1st SCS and a metal layer is formed on the insulating layer. Pref. a number of metal layers are formed on each substrate with the metal layers sepd. from each other and from the substrates by an insulating layer. Electrical connections are formed between at least 1 metal layer and the SCS. At least 1 metal layer consists of Ti or Al. Bonding is effected at 700-1,200 deg.C in an atmos. consisting of water vapour and O2. USE/ADVANTAGE - To produce

high density SC devices in which high density interacting patterns can be formed; a high degree of device insulation can be maintained.
(Dwg.1c/2)
US 5025304 A
Buried metal layer semiconductor device comprises: (i) first and second metal layers on substrate, with oxide bond between being thick enough to form insulation; (ii) second buried insulating layer on second buried metal layer; and (iii) semiconductor layer on second buried insulating layer. One or more vias connect buried metal layers to **active** devices in **substrate**. USE/ADVANTAGE - Used for formation of semiconductor and **integrated circuit** devices. Esp. for prodn. of semiconductor structure where high density devices and high density device interconnection patterns may be formed.
(6pp

7/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06099002
MANUFACTURE OF SEMICONDUCTOR **CHIP**

PUB. NO.: 11-040521 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): KOJIMA YOSHIKAZU
KAMIYA MASAAKI
APPLICANT(s): SEIKO INSTR INC
APPL. NO.: 10-097768 [JP 9897768]
FILED: April 09, 1998 (19980409)
PRIORITY: 09130164 [JP 979130164], JP (Japan), May 20, 1997 (19970520)

ABSTRACT

PROBLEM TO BE SOLVED: To improve scribe efficiency and to reduce **scribe line** width by forming a plurality of **integrated circuits**, on a wafer surface, in lattice through each **scribe line** for holding a **chip**, and moving a wire while it is made to contact the **scribe line**, for dicing.

SOLUTION: Wire rows running side by side in pitch of **scribe line** are made contact linearly the **scribe line** of a patterned wafer, and with an abrasive liquid supplied to the contact part, the wire is made to travel in one direction for cutting a **chip**. In short, a plurality of **integrated circuits** are patterned in matrix on a wafer surface. Between **integrated circuits**, a lattice-like **scribe line** is provided. A patterned wafer 18 is set on a wafer supporting stage 17. The wafer 18 is normally set on the wafer supporting stage 17 through a dummy plate 19. Then the wafer is scribed with a wire saw. Since a thin wire is used, a cut width can be narrower compared to using peripheral cutting edge saw.

7/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012867393
WPI Acc No: 2000-039226/**200003**
XRPX Acc No: N00-029559
Gate array **integrated circuit** fabricating and testing method with fast turn high performance function
Patent Assignee: LIGHTSPEED SEMICONDUCTOR CORP (LIGH-N)
Inventor: ELTOUKHY S; OSANN R
Number of Countries: 020 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9959207	A1	19991118	WO 99US10418	A	19990512	200003	B
US 6133582	A	20001017	US 9879016	A	19980514	200054	
US 6399400	B1	20020604	US 9879016	A	19980514	200242	
			US 99272470	A	19990319		

Priority Applications (No Type Date): US 9879016 A 19980514; US 99272470 A 19990319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9959207	A1	E	38	H01L-027/118	
Designated States (National): JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6133582	A			H01L-023/58	
US 6399400	B1			H01L-021/66	Div ex application US 9879016 Div ex patent US 6133582

Abstract (Basic): **WO 9959207** A1
Abstract (Basic):
NOVELTY - Performance test circuit is tested after suspension of fabrication technique, based on which, the wafers are assigned to performance bins. The wafers are allocated to customers requirements depending on customer's performance need. Then the previously protected active die area is etched to customize the wafer and final metal layer based on customer's design after resuming the fabrication technique.

DETAILED DESCRIPTION - Wafers consisting of generic function modules is fabricated. The performance testing circuit either in active die area or in **scribe line** area and their associated interconnection using totally available interconnection layers are fabricated from semiconductor fabrication technique. Photoresist is applied to completely protect the active die area prior to etching the top layer of metal for customizing the wafer for specific customer designs. The test circuits are etched to provide metal test points for probing the wafer to perform electrical speed test for binning purposes. Then the fabrication technique at this point is suspended.

USE - For fabricating and testing gate array DC with fast turn high performance function.

ADVANTAGE - Since the test circuits are individually tested on wafer by wafer bases, the performance data based on the test results of these test circuits can be very accurate for the wafer. Since the variation of the values of the parasitic elements, gains of active elements, and capacitance and inductance per unit length between dies on the same wafer tends to be reduced, the test results from the test

circuits gives accurate indication of the performance of the neighboring circuits.

DESCRIPTION OF DRAWING(S) - The figure shows flow chart illustrating the application of the fabricating method.

pp; 38 DwgNo 15/24

7/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012390317
WPI Acc No: 1999-196424/**199917**
XRPX Acc No: N99-144690
Semiconductor **chip** manufacturing method - involves dicing wafer by contacting wire to each **scribed line** and moving wire along each **scribed line**
Patent Assignee: SEIKO INSTR INC (DASE)
Inventor: KAMIYA M; KOJIMA Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11040521	A	19990212	JP 9897768	A	19980409	199917 B
US 6107163	A	20000822	US 9881987	A	19980520	200042 N

Priority Applications (No Type Date): JP 97130164 A 19970520; US 9881987 A 19980520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11040521	A		5	H01L-021/301	
US 6107163	A			H01L-021/46	

Abstract (Basic): JP 11040521 A
NOVELTY - **Integrated circuits** are formed on the wafer surface in the shape of a lattice via the **scribed lines**. A tape is bonded to the back-side of the wafer. A wire (14) is contacted to each **scribed line**. Dicing of the wafer is performed by moving the wire along each **scribed line**.
USE - For forming **integrated circuits** on wafer, and separating **integrated circuits**.
ADVANTAGE - Raises number of **integrated circuits** that can be formed on wafer and reduces scribe time by reducing **scribed-line** width. DESCRIPTION OF DRAWING(S) - The figure shows a schematic diagram explaining the scribe process. (14) Wire.
Dwg.1/5

7/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012049774
WPI Acc No: 1998-466684/**199840**
Related WPI Acc No: 1997-558109; 1999-493703
XRAM Acc No: C98-141474
XRPX Acc No: N98-363545
Horizontal and vertical **integrated circuit** wafer **scribe line** structures - with sloped sidewall of the line for increased yield
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: CARTER G N; CHAMBERS E A; DELGADO M A; DHAR R; RICHARDSON B D; VOKOUN E R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5795815	A	19980818	US 93176353	A	19931230	199840 B
			US 96699492	A	19960819	

Priority Applications (No Type Date): US 93176353 A 19931230; US 96699492 A 19960819
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5795815	A		15	H01L-021/301	Div ex application US 93176353 Div ex patent US 5686171

Abstract (Basic): US 5795815 A

A **scribe line** in multiple layers is formed by sequentially providing a plurality of alternating conductive and insulative layers (114,118,122,126) over a substrate (112), each layer with an elongated opening formed relative to the desired **scribe line** position. The opening in any layer are the same or wider than the preceding layer such that at least one sidewall of the **scribe line** has a slope outward from the base.

A final layer (134) seals the edges of the layers. The sloping sidewall reduces contamination problems and enhances planarisation during subsequent spin on material processes.

USE - Fabrication of **integrated circuits scribe lines**.

ADVANTAGE - The sloping wall on the **scribe line** increases yield by reducing problems with traps and spin on material build-up.

Dwg.7e/9

12/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013955991
WPI Acc No: 2001-440205/**200147**
XRPX Acc No: N01-325530
Fabrication method for **integrated circuit** involves forming **integrated circuit** on elements provided to common base by formation of grooves such that elements are separated along groove after circuit formation
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: FONG C S; HSU C S; TSENG C Y; WANG H T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6235612	B1	20010522	US 9888763	A	19980610	200147	B
			US 99324943	A	19990603		

Priority Applications (No Type Date): US 9888763 P 19980610; US 99324943 A 19990603
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6235612	B1		8	H01L-021/301	Provisional application US 9888763

Abstract (Basic): **US 6235612** B1
Abstract (Basic):
NOVELTY - The grooves (33,34) are formed to the surface of a wafer (30) to provide elements (32) on a common base. The circuit components, interconnections, and **bonding pads** are formed on the top surface of each element to form an **integrated circuit**. **Bonding pads** are also provided to the sides of each element. The **integrated circuits** are separated along the grooves.
USE - For fabricating **integrated circuits** with side wall contacts.
ADVANTAGE - Provides the necessary leads and contacts to the **integrated circuit** without any difficulty.
DESCRIPTION OF DRAWING(S) - The figure shows the isometric view of the semiconductor wafer.
Wafer (30)
Elements (32)
Grooves (33,34)
pp; 8 DwgNo 3/7

12/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013506687
WPI Acc No: 2000-678631/**200066**
Related WPI Acc No: 2002-290837
XRAM Acc No: C00-206293
XRPX Acc No: N00-502341

Fabrication of interconnect for semiconductor component, e.g. bare dice, by depositing, exposing, etching, and curing a polymer layer to form a raised contact member, and forming a conductive layer on the contact member

Patent Assignee: AKRAM S (AKRA-I); FARNWORTH W M (FARN-I)
Inventor: AKRAM S; FARNWORTH W M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6130148	A	20001010	US 97989444	A	19971212	200066	B

Priority Applications (No Type Date): US 97989444 A 19971212
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6130148	A		10	H01L-021/44	

Abstract (Basic): **US 6130148** A
Abstract (Basic):

NOVELTY - An interconnect is fabricated by depositing a resist on a substrate to form a polymer layer which is then exposed, etched, and cured to form a raised contact member on the substrate; and forming a conductive layer on the contact member to electrically engage the contact on the component. The resist is configured to form features with aspect ratio (height/width) of at least 10.

DETAILED DESCRIPTION - Fabrication of an interconnect for a semiconductor component having a contact comprises depositing a resist on a substrate (10) to form a polymer layer (14); exposing, etching, and curing the polymer layer to form a raised contact member (26) on the substrate, and forming a conductive layer (34) on the contact member configured to electrically engage the contact on the component. The resist is configured to form features with an aspect ratio (height/width) of at least 10.

USE - The method is useful for the fabrication of an interconnect useful for electrically contacting semiconductor components, e.g., bare dice, wafers and **chip** scale packages.

ADVANTAGE - The method provides electrical connections having a low contact resistance and which can cause minimal damage to the device **bond pads** or external contacts.

DESCRIPTION OF DRAWING(S). - The figures are cross-sectional views illustrating the fabrication of the interconnect.

Substrate (10)
Insulating layer (12)
Polymer layer (14)
Projections (20)
Contact member (26)
Conductive layer (34)
pp; 10 DwgNo 1C, 1F/7

12/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009996658
WPI Acc No: 1994-264369/**199432**
XRPX Acc No: N94-207956
Circuit assembly fabrication method esp. for multilayered three-dimensional **integrated circuit** - forming vertical feedthroughs in SOI **IC** to underlying insulator, bonding temporary substrate to wafer upper surface, thinning SOI wafer to insulator, and forming bump **bonding pads** for top and bottom interconnects
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: FINNILA R M
Number of Countries: 018 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9417553	A1	19940804	WO 94US363	A	19940110	199432	B
EP 631692	A1	19950104	EP 94906589	A	19940110	199506	
			WO 94US363	A	19940110		
US 5426072	A	19950620	US 936601	A	19930121	199530	
JP 7506936	W	19950727	JP 94517067	A	19940110	199538	
			WO 94US363	A	19940110		

Priority Applications (No Type Date): US 936601 A 19930121
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9417553	A1	E	34	H01L-025/065	
Designated States (National): JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 631692	A1	E	2	H01L-025/065	Based on patent WO 9417553
Designated States (Regional): FR GB					
US 5426072	A		12	H01L-021/283	
JP 7506936	W		11	H01L-027/00	Based on patent WO 9417553

Abstract (Basic): WO 9417553 A

The circuit fabrication process involves processing a multilayered wafer with a semiconductor material layer over a dielectric layer on a silicon substrate surface, to form one or more feedthrough conductors and circuitry within the semiconductor layer. The feedthroughs may be thick film or thin film. An interconnect is formed over the semiconductor layer, connected to the feedthrough(s). A temporary substrate is attached to the assembly, on the interconnect and opposite the semiconductor layer.

The silicon substrate is removed, by etching e.g. either in a KOH soln. or by plasma etching, to expose the dielectric layer. Pref. an etch protective material is used at the multilayered wafer edge. Additional interconnect is formed through the dielectric, for coupling to the feedthrough(s). The interconnects are pref. formed with an or solder indium bump aligned and connected to the feedthrough(s). The temporary substrate may be removed and two similar assemblies stacked, with interconnection through respective bumps.

USE/ADVANTAGE - In wafer stack or sawn into die after stacking. Supports bipolar, MOS and combined technologies; high circuit density with small vertical feedthrough.

Dwg.5/10

Abstract (Equivalent): US 5426072 A

A method of mfg. integrated three-dimensional i.c's involves initially providing a first and a second silicon-on-insulator (SOI) wafer, wherein each SOI wafer includes a silicon layer separated from a bulk silicon substrate by a layer of dielectric material, typically SiO2. Next, at least one electrical feedthrough is formed in each of the silicon layers and active and passive devices are formed in each of the thin silicon layers. Then interconnects are formed that overlie the silicon layer and are electrically coupled to the feedthrough. One of the wafers is then attached to a temporary substrate, such that the interconnects are interposed between the thin silicon layer and the temporary substrate.

The bulk silicon substrate of the wafer having the temporary substrate is then etched to expose the dielectric layer. Further interconnects are then formed through the exposed dielectric layer for electrically contacting the at least one feedthrough. This results in the formation of a first circuit assembly. A next step then couples the further interconnects of the circuit assembly to the interconnects of the second SOI wafer, the second SOI wafer having a bulk substrate, a dielectric layer overlying a surface of the substrate, and a layer of processed silicon overlying the dielectric layer. The temporary substrate is then removed. Additional circuit assemblies may then be stacked and interconnected to form a three-dimensional **integrated circuit**.

USE/ADVANTAGE - **Integrated circuit** mfg. technology. Small volume i.c's providing three-dimensional circuits that support MOS, bipolar, or combination technologies.

Dwg.5,6/10

12/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009838843
WPI Acc No: 1994-118699/**199414**
XRPX Acc No: N94-092942
High yield fabrication of **IC** devices on silicon wafer - includes slicing process that defines a number of **IC** elements and exposes sectional surfaces of multiplicity of pads
Patent Assignee: BADEHI P (BADE-I); SHELLCASE LTD (SHEL-N)
Inventor: BADEHI P; PIERRE B
Number of Countries: 043 Number of Patents: 017
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9407267	A1	19940331	WO 92EP2134	A	19920914	199414	B
ZA 9306039	A	19940525	ZA 936039	A	19930818	199424	
PT 101354	A	19940729	PT 101354	A	19930902	199429	

Priority Applications (No Type Date): WO 92EP2134 A 19920914; TW 94110998 A 19930217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9407267	A1	E	45	H01L-025/065	

Designated States (National): AT AU BB BG BR BY CA CH CS DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO PL RO RU SD SE US
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL OA SE

ZA 9306039	A	47	H01L-000/00	
PT 101354	A		H01L-021/00	
AU 9225541	A		H01L-025/065	Based on patent WO 9407267

Abstract (Basic): WO 9407267 A

The device structure includes a relatively thin and compact **IC** package (10) having electrical contacts (12) plated along the edge surfaces (14), to extend onto the planar surfaces (16) of the package. Integral ground plane contacts (18) are provided, together with thermal **bonding pads** (19) on the planar surfaces.

During fabrication, a number of ICs are produced on each wafer having two planar surfaces and a multiplicity of pads which are sliced so as to simultaneously define electrical contact regions for both of a pair of adjacent ICs. This contact arrangement permits both flat surface mounting and edge mounting onto a circuit board.

ADVANTAGE - Provides devices with relatively smaller size and weight, and enhanced electrical performance, and overcomes prior problems of thermal expansion mismatch.

Dwg.1/12

Abstract (Equivalent): US 5547906 A

A method of producing prepackaged **integrated circuit** devices comprising the steps of:

providing a wafer having a first surface and a second surface generally parallel to and oppositely directed with respect to said first surface;

producing a plurality of **integrated circuit** dies on said first surface of said wafer, each of the **integrated circuit** dies comprising a multiplicity of pads;

attaching a first electrically insulative plate to said plurality

of **integrated circuit** dies on the first surface of said wafer;

separating the **integrated circuit** dies from each other so as to define edges thereof while the dies remain attached to the insulative plate;

generally surrounding said **integrated circuits** on said edges and said second surface with a protective sealant; and

thereafter slicing the wafer and protective sealant and the insulative plate attached thereto, thereby to define a plurality of prepackaged **integrated circuit** devices.

4A,4E/12B

12/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009823412
WPI Acc No: 1994-103268/**199413**
XRAM Acc No: C94-047551
Hermetically sealed **IC** - includes a PVD or CVD ceramic sealing layer which also covers the sidewalls of a prim. passivation layer and **bond pad** and street sites
Patent Assignee: MICHAEL K W (MICH-I); DOW CORNING CORP (DOWO)
Inventor: MICHAEL K W; KEITH WINTON M
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 589678	A2	19940330	EP 93307461	A	19930921	199413	B
CA 2106694	A	19940324	CA 2106694	A	19930922	199423	
JP 6204282	A	19940722	JP 93236014	A	19930922	199434	
TW 232095	A	19941011	TW 93107683	A	19930920	199445	
EP 589678	A3	19950412	EP 93307461	A	19930921	199544	
US 5825078	A	19981020	US 92948570	A	19920923	199849	

Priority Applications (No Type Date): US 92948570 A 19920923
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 589678	A2	E	6	H01L-023/02	
Designated States (Regional): DE FR GB IT NL					
JP 6204282	A		5	H01L-021/60	
CA 2106694	A			H01L-023/29	
TW 232095	A			H01L-023/28	
EP 589678	A3			H01L-023/02	
US 5825078	A			H01L-023/58	

Abstract (Basic): EP 589678 A

IC comprises: a circuit assembly with **bond pads**; a prim. passivation layer which is etched at the **bond pads** and streets; and one more ceramic layers covering the prim. passivation layer including the sidewalls created by etching at the pads and streets, the ceramic layer(s) being PVD or CVD layers.

A non-corroding conductive layer, pref. of Au, Ag, W, solder, Cu or Ag-filled epoxy, is included on the **bond pads**. A diffusion barrier layer on the pads may also be included. The ceramic layer(s) are formed of ceramics based on Si, SiO, SiN, SiON, SiOC, SiCN, SiOCN, SiC or diamond-like C materials. The diffusion barrier layer is pref. Ti, TiW or TiN. The device may be encapsulated in an organic or silicone encapsulant.

ADVANTAGE - The PVD or CVD ceramic layer(s) provide sealing of enhanced hermeticity esp. at the pads and streets.

Dwg.0/2

28aug03 09:50:47 User267149 Session D950.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2003/Aug W3
(c) 2003 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2003/Aug W4
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*File 6: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 8:Ei Compendex(R) 1970-2003/Aug W3
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*File 8: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 34:SciSearch(R) Cited Ref Sci 1990-2003/Aug W4
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
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(c) 2003 INIST/CNRS
File 305:Analytical Abstracts 1980-2003/Aug W1
(c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2003/Jul
(c) 2003 DECHEMA
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200355
(c) 2003 Thomson Derwent
File 347:JAPIO Oct 1976-2003/Apr(Updated 030804)
(c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Mar
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

AUTHOR

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Set     Items   Description
S1     108485   AU=(LEE, J? OR LEE J?)
S2      10232   AU=(LIN, M? OR LIN M?)
S3         30   S1 AND S2
S4          0   S3 AND PLANAR???????(3N)INDUCT??????
S5         10   S3 AND ((INTEGRAT????????(3N)(CIRCUIT???????? OR LOOP? ?))
               OR IC OR CHIP? ?)
S6          0   S5 AND REGION? ?(3N)(ACTIV???????? OR PASSIV????????)
S7         10   RD S5 (unique items)
S8         20   S3 NOT S7
S9          0   S8 AND GLASS(3N)(PANEL? ? OR PASSIV?????????)
S10         0   S8 AND (CUTTING OR CUT OR SLICE???? OR INCISE???? OR REMOV-
              ??????? OR PENETRAT???????)(3N)SUBSTRATE? ?
?
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7/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06452534
E.I. No: EIP03297550237
Title: A new system-on-a-**chip** (SOC) technology - High Q post passivation inductors
Author: Chen, Ling; Chou, Kevin; Hsiao, Roger; Lin, Eric; **Lin, M.S.**; **Lee, J.Y.**; Wan, K.H.; Chen, H.M.
Corporate Source: Megic Corp, Hsinchu Sci. Indust. Park, Hsinchu, Taiwan
Conference Title: 53rd Electronic Components and Technology Conference 2003
Conference Location: New Orleans LA, United States Conference Date: 20030527-20030530
E.I. Conference No.: 61145
Source: Proceedings - Electronic Components and Technology Conference 2003. p 1503-1509 (IEEE cat n 03CH37438)
Publication Year: 2003
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: This paper presents a new SOC scheme by adding high Q (greater than 15) inductors on top of **IC** passivation layer. Affiliated with such a high Q inductor, a high performance RF CMOS **chip** can be achieved, which may replace some applications of GaAs **chips**. The high Q value of the inductor is attributed to the large gap formed by the thick polyimide located between the inductor body and **IC** passivation layer, as well as the thick metal traces of inductors. Conventional **IC** front-end process technology cannot offer these advantages as it places the inductor closer to the silicon substrate, and its metal is thinner than 2 mu m. The manufacturing cost of post-passivation inductor is also much lower than that of font-end **IC** process in that the post passivation inductors can be fabricated in a more relaxed manufacturing environment Two kinds of inductor bodies, copper and gold, have been developed, respectively. At 5 GHz, the post passivation inductor demonstrated a Q factor as high as 24, which is much greater than that of the ones formed by **IC** front-end process that are positioned under the passivation layer (Q value lower than 10). The reliability results of the new SOC scheme will be also presented. 10 Refs.

7/3,AB/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02720462
E.I. Monthly No: EI8903019282
Title: Implementation of array structured maximum likelihood decoders.
Author: Wen, Kuei-Ann; Wang, Jhing-Fa; **Lee, Jau-Yien; Lin, Ming-Yung**
Corporate Source: Natl Cheng Kung Univ, Tainan, Taiwan
Conference Title: Proceedings - International Conference on Systolic Arrays.
Conference Location: San Diego, CA, USA Conference Date: 19880525
E.I. Conference No.: 11793
Source: Proc Int Conf on Systolic Arrays. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (cat n 88CH2603-9) Piscataway, NJ, USA. p 227-236
Publication Year: 1988
ISBN: 0-8186-8860-2
Language: English
Abstract: Efficient VLSI array processor architectures for maximum-likelihood decoding (MLD) have been developed to meet the high throughput and data processing requirements of modern communication systems. Both 1-D and 2-D MLD processors with large constraint length (greater than 8) have been derived. Radix-4p processing elements and delay-commutating switching processors for MLD have been concatenated to construct a pipeline MLD processor. The pipeline length can be adapted to meet the time/area constraints for various applications. A 2-D MLD array processor is also presented. Processing data are modulized, data transmissions are embedded into processing elements, and a fixed-size 2-D MLD array is derived to meet high-data-throughput requirements. 22 Refs.

7/3,AB/3 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04641552 INSIDE CONFERENCE ITEM ID: CN048502489
A New System-on-a-**Chip** (SOC) Technology: High Q Post Passivation Inductors
Lin, M. S.; Chen, L.; **Lee, J. Y.**; Wan, K. H.; Chen, H. M.; Chou, K.; Hsiao, R.; Lin, E.
CONFERENCE: Electronic components and technology conference-53rd
ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE, 2003; 53RD P: 1503-1509
IEEE, 2003
ISSN: 0569-5503 ISBN: 0780379915
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: Institute of Electrical and Electronics Engineers
CONFERENCE LOCATION: New Orleans, LO 2003; May (200305) (200305)

7/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015449647
WPI Acc No: 2003-511789/200348
XRPX Acc No: N03-406128
Chip packaging structure and manufacturing process of the same - capable of integrating the **chips** having the same function or different functions inside the same packaging body such that the **chips** can be electrically connected wi
Patent Assignee: MEGIC CORP (MEGI-N); HUANG C (HUAN-I); LEE J (LEEJ-I); LIN M (LINM-I)
Inventor: HUANG J; LI J; **LIN M**; HUANG C; **LEE J**
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 503496	A	20020921	TW 2001133195	A	20011231	200348	B
US 20030124835	A1	20030703	US 200255568	A	20020122	200351	
			US 2002174462	A	20020617		
US 20030122246	A1	20030703	US 200255568	A	20020122	200351	

Priority Applications (No Type Date): TW 2001133195 A 20011231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 503496	A			H01L-021/60	
US 20030124835	A1			H01L-023/522	Div ex application US 200255568
US 20030122246	A1			H01L-021/48	

Abstract (Basic): TW 503496 A
Abstract (Basic):
NOVELTY - A **chip** packaging structure and its manufacturing process are disclosed in the present invention. In the invention, a **chip** is adhered to a silicon substrate, and a multi-layered circuit layer is formed on the **chip** and the silicon substrate. The multi-layered circuit layer has an external circuit that is electrically connected with the metal pad on the **chip**, and part of the external circuit is extended to the region excluding the upper side of the **chip**'s active surface for fanning out the metal pads

of the **chip**. In addition, an internal circuit and multiple active devices are provided on the **chip**'s active surface, in which signals can be transmitted from an active device to the external circuit through an internal circuit, and then transmitted from the external circuit to the other active device through the internal circuit. Furthermore, for the invention, it is capable of integrating the **chips** having the same function or different functions inside the same packaging body such that the **chips** can be electrically connected with each other through the external circuit.

DwgNo 1/1

7/3,AB/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015105281
WPI Acc No: 2003-165798/200316
XRAM Acc No: C03-042966
XRPX Acc No: N03-130911

Chip scale package for **integrated circuit** comprises ball mountings formed over adsubstrate, reaching under-ball metallurgy layer over input/output pads on **chip**

Patent Assignee: MEGIC CORP (MEGI-N)
Inventor: HUANG C; **LEE J**; **LIN M**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020140069	A1	20021003	US 2001821546	A	20010330	200316	B

Priority Applications (No Type Date): US 2001821546 A 20010330
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020140069	A1		15	H01L-021/44	

Abstract (Basic): US 20020140069 A1
Abstract (Basic):

NOVELTY - A **chip** scale package has a silicon **chip** (100) having input/output (I/O) pads, an under-ball metallurgy (UBM) layer on the surface of I/O pads, a substrate (150) (adsubstrate) with an adhesive, and ball mountings (190). The substrate has openings corresponding to the locations of the I/O pads. The ball mountings are formed over the adsubstrate and reach the UBM layer over the I/O pads on the **chip**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for formation of a **chip** scale package. An adhesive layer (160) is formed on the substrate to form an adsubstrate composite. The openings are formed in the adsubstrate composite, and the **chip**(s) are attached on the adsubstrate composite where the I/O pads of the **chip**(s) are placed on the corresponding openings on the adsubstrate composite to form a package. A molding material (180) is formed around the package. The ball mounting are formed over the openings on the adsubstrate of the package to form **chip** scale package.

USE - **Chip** scale package for high frequency circuit applications.

ADVANTAGE - The **chip** scale package provides integrated and short **chip** connections, improves testing cost, and has minimized

interconnection lengths and thus enhanced circuit speed. The thermal reliability of the package is improved and the coefficient of thermal expansion mismatch between silicon **chip** and next level of packaging is reduced by encapsulating the **chips** with molding material. The performance of various levels of packaging in computers is improved by the solder connections.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section view of a portion of the **chip** scale package.

Chip (100)
Substrate (150)
Adhesive layer (160)
Molding material (180)
Ball mountings (190)
pp; 15 DwgNo 2i/4

7/3,AB/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015077896
WPI Acc No: 2003-138414/200313
Related WPI Acc No: 2002-290796; 2002-396715; 2002-555993; 2002-573700; 2003-102186; 2003-310482; 2003-391059; 2003-539681
XRAM Acc No: C03-035140
XRPX Acc No: N03-109786

Chip structure, comprises substrate, first and second build-up layers, and passivation layer

Patent Assignee: HUANG C (HUAN-I); LEE J (LEEJ-I); LIN M (LINM-I)
Inventor: HUANG C; **LEE J**; **LIN M**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020109232	A1	20020815	US 98216791	A	19981221	200313 B
			US 99251183	A	19990217	
			US 2000691497	A	20001018	
			US 2001972639	A	20011009	
			US 2002124388	A	20020415	

Priority Applications (No Type Date): US 2002124388 A 20020415; US 98216791 A 19981221; US 99251183 A 19990217; US 2000691497 A 20001018; US 2001972639 A 20011009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020109232	A1		30	H01L-023/48	CIP of application US 98216791
					CIP of application US 99251183
					CIP of application US 2000691497
					CIP of application US 2001972639
					CIP of patent US 6383916

Abstract (Basic): US 20020109232 A1
Abstract (Basic):

NOVELTY - A **chip** structure comprises a substrate having electric devices that are disposed on substrate surface; first build-up layer located on the substrate surface; a passivation layer disposed on the first built-up layer; and a second built-up layer arranged over the passivation layer.

DETAILED DESCRIPTION - A **chip** structure comprises:

(i) a substrate having electric devices that are disposed on substrate surface;

(ii) first build-up layer located on the substrate surface;

(iii) a passivation layer disposed on the first built-up layer; and

(iv) a second built-up layer arranged over the passivation layer.

The first built-up layer includes a dielectric body and a first interconnection scheme. The first interconnection scheme interlaces inside the dielectric body of the first built-up layer and is electrically connected to the electric devices.

The passivation layer is provided with an opening(s) exposing the first interconnection scheme. The second built-up layer is provided with a second interconnection scheme.

The second interconnection scheme electrically connected to the first interconnection layer with passing through the opening of the passivation layer. The trace thickness of the second interconnection scheme is larger than that of the first interconnection scheme.

A signal is transmitted from one of the electric devices to the first interconnection scheme, then passes through the passivation layer, and finally is transmitted to the second interconnection scheme. It also transmitted from the second interconnection scheme to the first interconnection scheme with passing through the passivation layer, and is finally transmitted to the electric device.

An INDEPENDENT CLAIM is included for a process of fabricating a **chip** structure comprising providing a wafer with electric devices, an interconnection scheme and a passivation layer.

Both the electric devices and the interconnection scheme are arranged inside the wafer. The interconnection scheme is electrically connected with the electric devices. The passivation layer is disposed on layer surface of the wafer.

The passivation layer has an opening exposing the interconnection scheme. A conductive layer is formed over the passivation layer of the wafer and is conductive layer electrically connected with the interconnection scheme. A photoresist is formed onto the conductive layer. The photoresist has an opening exposing the conductive layer. A conductive metal(s) (680) is filled over the conductive layer. The photoresist is removed. The conductive layer not covered with the conductive metal is removed.

USE - Used as **chip** structure.

ADVANTAGE - The invention improves resistance-capacitance delay and reduces energy loss of the **chip**. The production cost of the **chip** structure can be reduced and the circuit layout can be simplified.=

DESCRIPTION OF DRAWING(S) - The figure is cross-sectional view of fabricating a **chip** structure.

Node opening (672)

Conductive metal (680)

pp; 30 DwgNo 22/22

7/3,AB/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015041670
WPI Acc No: 2003-102186/200309
Related WPI Acc No: 2002-290796; 2002-396715; 2002-555993; 2002-573700; 2003-138414; 2003-310482; 2003-391059; 2003-539681
XRAM Acc No: C03-025640

XRPX Acc No: N03-081599
Chip structure, used in electronic equipment, includes substrate having electrical devices, first built-up layer including dielectric body and second built-up layer
Patent Assignee: MEGIC CORP (MEGI-N); HUANG C (HUAN-I); LEE J (LEEJ-I); LIN M (LINM-I)
Inventor: HUANG J; LI J; **LIN M**; HUANG C; **LEE J**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020115282	A1	20020822	US 98216791	A	19981221	200309 B
			US 99251183	A	19990217	
			US 2000691497	A	20001018	
			US 2001972639	A	20011009	
			US 2002125226	A	20020416	
TW 511243	A	20021121	TW 2001131030	A	20011214	200353

Priority Applications (No Type Date): TW 2001131796 A 20011221; TW 2001130876 A 20011213; TW 2001131030 A 20011214
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020115282	A1		32	H01L-021/4763	CIP of application US 98216791
					CIP of application US 99251183
					CIP of application US 2000691497
					CIP of application US 2001972639
					CIP of patent US 6383916
TW 511243	A			H01L-021/768	

Abstract (Basic): US 20020115282 A1
Abstract (Basic):
NOVELTY - A **chip** structure comprises a substrate having electrical devices, a first built-up layer including a dielectric body and a first interconnection scheme, and a second built-up layer arranged on the first built-up

DETAILED DESCRIPTION - A **chip** structure comprises a substrate having electrical devices on its surface. A first built-up layer is located on the substrate including a dielectric body and a first interconnection scheme interlacing inside its dielectric body. The first interconnection scheme is electrically connected to the electric devices, and includes two conductive pad(s). The conductive pads are located on the first built-up layer, and the first conductive pad is exposed to the outside. A second built-up layer is on the first built-up layer. It is provided with a second interconnection scheme which is electrically connected with the first interconnection layer through the second conductive pad.

An INDEPENDENT CLAIM is included for a method for the fabrication of a **chip** structure comprising:

(a) providing a wafer with a passivation layer;

(b) forming a dielectric sub-layer having an opening(s) (772), on the passivation layer;

(c) forming a conductive metal(s) (780) on the dielectric sub-layer and into the opening; and

(d) removing the conductive metal formed outside the opening.

USE - Used in electronic equipment.

ADVANTAGE - Improved resistance-capacitance delay and a reduced energy loss. It can be produced using facilities with low accuracy so production costs can be reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the

chip structure.
Second conductive sub-layer (741, 770)
Opening (772)
Conductive metal (780)
pp; 32 DwgNo 23/26

7/3,AB/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014956610
WPI Acc No: 2003-017124/200301
XRAM Acc No: C03-004100
XRPX Acc No: N03-013024
Solder bump formation in semiconductor **integrated circuit** device manufacture, involves providing pillar metal and under bump metal layers between contact pads and solder bumps
Patent Assignee: MEGIC CORP (MEGI-N)
Inventor: HUANG C; **LEE J**; **LIN M S**; **LIN M**
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020121692	A1	20020905	US 2001798654	A	20010305	200301	B
EP 1239514	A2	20020911	EP 2002392002	A	20020305	200301	

Priority Applications (No Type Date): US 2001798654 A 20010305
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020121692	A1		17	H01L-021/44	
EP 1239514	A2	E		H01L-021/60	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): US 20020121692 A1
Abstract (Basic):
NOVELTY - A barrier layer (35) is deposited on a substrate (10) having contact pads (32) with passivation layers (34) in between. A photoresist layer exposing the contact pad is formed and pillar metal, under the bump metal and solder metal layers (38, 40, 42), are sequentially formed in the exposed area. The photoresist layer is removed and the metal layers are etched suitably. The solder metal is reflown to form a solder bump.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a solder bump.
USE - For forming solder bumps (claimed) during the manufacture of semiconductor **integrated circuit** devices.
ADVANTAGE - A fine pitch solder bump of high reliability is provided by increasing the height of the solder bump, thereby preventing thermal mismatch between the overlying layers of a semiconductor package.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the solder bump.
Substrate (10)
Contact pad (32)
Passivation layer (34)
Barrier layer (35)
Pillar metal layer (38)

Bump metal layer (40)
Solder metal layer (42)
pp; 17 DwgNo 16/16

7/3,AB/9 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014912093
WPI Acc No: 2002-732799/200279
XRPX Acc No: N02-577824
Apparatus for diagnosing failures in an **integrated circuit** using design-for-debug (DFD) techniques, a DFD selector indicates which scan cores and fault types will be debugged or diagnosed simultaneously
Patent Assignee: CHANG M (CHAN-I); CHAO H (CHAO-I); HSU C (HSUC-I); HSU P (HSUP-I); KAO S (KAOS-I); LEE J (LEEJ-I); LIN M (LINM-I); LIN S (LINS-I); TSAI S (TSAI-I); WANG H (WANG-I); WANG L (WANG-I); WEN X (WENX-I); SYNTEST TECHNOLOGIES INC (SYNT-N)
Inventor: CHANG M; CHAO H; HSU C; HSU P; KAO S; **LEE J**; **LIN M**; LIN S; TSAI S; WANG H; WANG L; WEN X
Number of Countries: 040 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200271567	A1	20020912	WO 2002US3413	A	20020228	200279 B
US 20020138801	A1	20020926	US 2001272064	A	20010301	200279
			US 200286214	A	20020227	

Priority Applications (No Type Date): US 200286214 A 20020227; US 2001272064 P 20010301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200271567	A1	E	92	H02H-003/05	
	Designated States (National): AU BR CA CN CZ ID IL IN JP KP KR MX NO NZ PL RO SG US VN ZA				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GR IE IT LU MC NL PT SE TR				
US 20020138801	A1			G01R-031/28	Provisional application US 2001272064

Abstract (Basic): WO 200271567 A1
Abstract (Basic):
NOVELTY - A DFD selector indicates which scan cores and selected fault types will be debugged or diagnosed simultaneously. A scan connector connects several scan chains in the scan cores to a boundary-scan chain in an **integrated circuit**. A scan clock generator generates an ordered sequence of capture clocks for connection to the scan clocks in the cores. A multiplexer connects the DFD selector and the scan controller to a TAP (test access port) controller in the circuit.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method for debugging or diagnosing several scan cores in an **integrated circuit**.
USE - In semiconductor manufacturing.
ADVANTAGE - Facilitates prototype debug and diagnosis using a low-cost DFT debugger.
DESCRIPTION OF DRAWING(S) - The drawing lists a number of boundary-scan controlled commands, including 14 basic design-for-debug (DFD) commands of one embodiment of the invention, for testing,

debugging or diagnosing scan cores, memory BIST cores, logic BIST cores and functional cores in an **integrated circuit**
pp; 92 DwgNo 1/20

7/3,AB/10 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014576011
WPI Acc No: 2002-396715/200243
Related WPI Acc No: 2002-290796; 2002-555993; 2002-573700; 2003-102186; 2003-138414; 2003-310482; 2003-391059; 2003-539681
XRPX Acc No: N02-311156
Post passivation interconnect structure for **integrated circuit** devices, uses thick wide metallization structure formed above passivation layer, as electrical stimulus distribution network
Patent Assignee: MEGIC CORP (MEGI-N); MAGIC CORP (MAGI-N)
Inventor: **LIN M; LEE J**
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1199750	A2	20020424	EP 2001480077	A	20010827	200243	B
US 6495442	B1	20021217	US 2000691497	A	20001018	200307	
US 20030057531	A1	20030327	US 2000691497	A	20001018	200325	
			US 2002278106	A	20021022		
SG 96209	A1	20030523	SG 20011847	A	20010323	200347	

Priority Applications (No Type Date): US 2000691497 A 20001018; US 2002278106 A 20021022
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1199750	A2	E	17	H01L-023/50	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
US 6495442	B1			H01L-021/4763	
US 20030057531	A1			H01L-023/495	Div ex application US 2000691497 Div ex patent US 6495442
SG 96209	A1			H01L-023/50	

Abstract (Basic): EP 1199750 A2
Abstract (Basic):
NOVELTY - A thick, wide metallization structure is formed over a passivation layer which is formed on a fine line metallization structure on a substrate. The thick wide metallization structure is connected to ESD and internal circuits and is used as an electrical stimulus distribution network.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of forming post passivation interconnection.
USE - In manufacture of **integrated circuit** devices.
ADVANTAGE - Fine line interconnect metal is created using methods of sputter with resist etching. fine line interconnect lines are created in a layer of inorganic dielectric, thick, wide interconnect lines are created in a layer of dielectric comprising polymer. This avoids development of fissures and cracks.
DESCRIPTION OF DRAWING(S) - The figure shows a cross section of silicon substrate over which interconnect structure is created.
pp; 17 DwgNo 3A/7